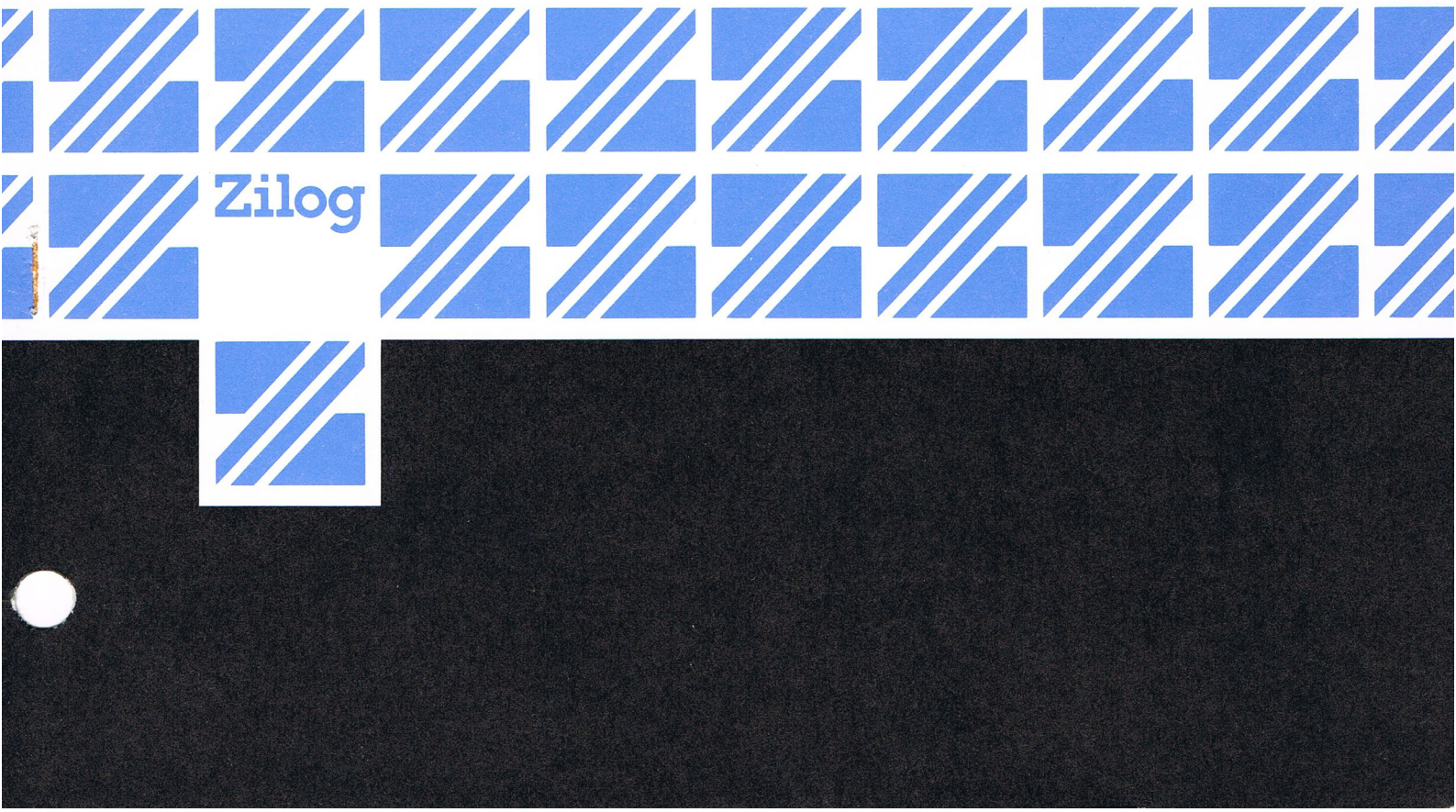
Z-80® MDC (MDC/E)

Hardware User's Manual



Price: 4.50
03-3006-01
Rev. B
August 1978

READER'S COMMENTS

Your feedback about this document is important to us: only in this way can we ascertain your needs and fulfill them in the future. Please take the time to fill out this questionnaire and return it to us. This information will be helpful to us, and, in time, to the future users of Zilog systems. Thank you.

Your Name: _____

Company Name: _____

Address: _____

Title of this document: _____

What software products do you have? _____

_____

_____

What is your hardware configuration (including memory size)? _____

_____

_____

Does this publication meet your needs? ☐ Yes ☐ No

If not, why not? _____

_____

_____

How do you use this publication? (Check all that apply)

- ☐ As an introduction to the subject?
- ☐ As a reference manual?
- ☐ As an instructor or student?

How do you find the material?

	Good	Fair	Poor
Technicality	☐	☐	☐
Organization	☐	☐	☐
Completeness	☐	☐	☐

What would have improved the material? _____

_____

_____

Other comments, suggestions or corrections: _____

_____

_____

If you found any mistakes in this document, please let us know what and where they were:

_____

_____

First Class

Permit No. 475
Cupertino
California
95014

Business Reply Mail

No Postage Necessary if Mailed in the United States

Postage Will Be Paid By

Zilog
Software Department Librarian
10460 Bubb Road
Cupertino, California 95014

MDC (MDC/E) HARDWARE USER'S MANUAL

TABLE OF CONTENTS

REVISION "B"
AUGUST 1978

1.0 INTRODUCTION

The Zilog Z80-MDC (Memory Disk Controller) and the MDC/E (European Version) are part of the Zilog MCB Series of OEM cards and systems. The MDC directly interfaces to all other boards in the MCB Series and provides optional 12K, 16K, 32K, or 48K bytes of dynamic RAM memory for program or data storage plus a floppy disk controller that is capable of handling up to eight floppy disk drives. The 12K version (assembled with 4K dynamic RAM devices) is separated into three pages of 4K bytes each. The starting address for each of the 4K byte pages may be set by programmable read only memory (PROM) to begin on any of up to 16 page boundaries. The other three versions are assembled using 16K dynamic RAM devices. For each version, the address decode PROM determines the starting address for the four segments of the 64K address space. The standard version, for which the following discussion applies, consists of 16K bytes.

A block diagram of the complete board is shown in Figure 1. A voltage converter is included on the board to convert the signal +5 volt input to the +12 and -5 volts required by the dynamic memory array. The upper address bits from the CPU are provided to a memory page decoder PROM. The starting address for each of the 16K byte memory banks can be set to any of four possible starting locations. The page decoder output is then supplied, along with A0 through A13, to a memory address multiplexer to provide the proper address signals, along with the CAS and RAS control signals, to the memory array. The memory array utilizes 16-pin, 16K-bit dynamic RAMs; although strapping options allow 4K-bit RAMs to also be used. The data that is written to or read from the memory is passed through the set of data bus buffers.

The bottom half of the diagram is the disk controller. This disk controller is very simple as all of the disk formatting and control is actually provided by the CPU under program control. The Z80-PIO is used by the Z80-CPU to latch disk control information and to sample disk status information. Thus, control and status information from the disk is passed between the CPU and the disk via the Z80-PIO. The data handling is provided by the blocks in the bottom part of the diagram. Data from the disk is provided to a data separator where the clock and data are separated into two distinct signals.

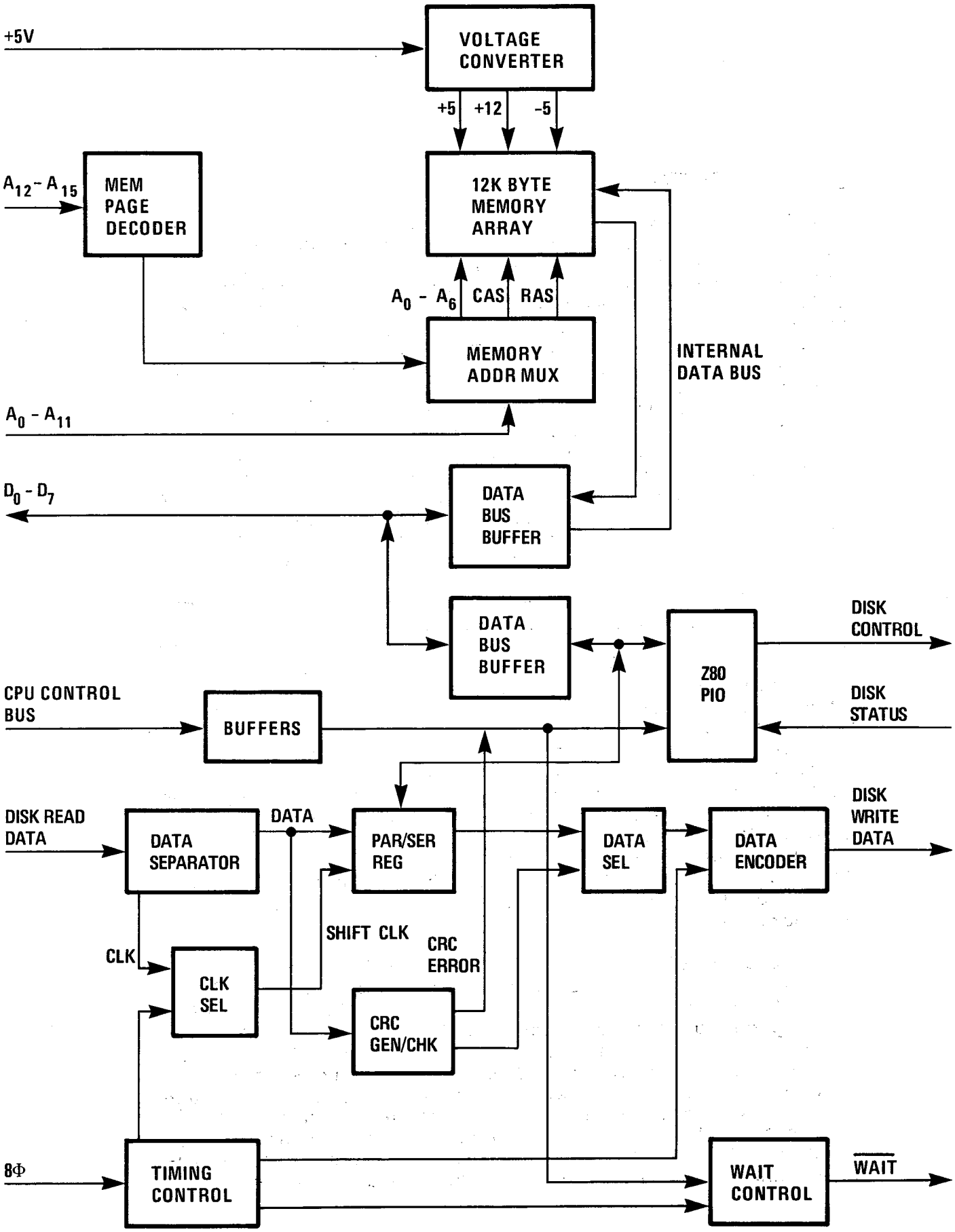


FIGURE 1
MDC BLOCK DIAGRAM

During READ operations, this data is then fed into the parallel/serial register. The shift clock during this operation is provided by the separated clock. While data is being supplied to the register, it is also being supplied to the CRC circuit. This CRC circuit generates a 16-bit cyclic redundancy check code which is used by the CPU to insure that data is correctly written onto and read back from the disk. Once a complete 8-bit byte has been assembled in the parallel/serial register, it is then read out to the CPU via the data bus buffers during a CPU I/O READ operation. The WAIT control logic synchronizes the speed of the CPU to the disk read speed by setting the CPU WAIT line to an active state until a complete byte of data has been assembled. Once a complete sector of data has been read from the disk, the CPU can then check to see if the CRC was correct by reading the CRC error bit from the CRC circuitry.

During WRITE operations, data is loaded via the data bus buffers into the parallel/serial register. From there, it is shifted out through the data multiplexer and to the data encoder where it is properly formatted for writing onto the disk. The timing for this is provided by the timing control circuit. This circuit uses the 8 PHI clock from the MCB Board to generate a shift clock for the register and to provide other timing signals to properly encode the data. Again, during this operation, a WAIT control is used to synchronize the CPU to the proper disk operating speed.

2.0 DETAILED DESCRIPTION OF BOARD SCHEMATICS

The following sections describe in detail the function of each separate sheet of the MDC Board Schematics.

2.1 Power Supply and Control Buffers

This sheet contains the DC to DC voltage converter which is used to convert the +5 power input to the -5 and +12 voltages which are required for the memory. Also contained on this sheet are bus buffers to isolate the CPU control signals and selected address bits from the system bus.

2.2 Memory Address Multiplexer

Sheet 2 contains the control logic for the memory page decoders and memory address multiplexer. The 74LS75 circuit latches the four upper address bits from the CPU during MREQ-. The 7603 PROM decodes these bits into four possible memory segment-selects allowing the user to select the starting locations for the memory. These selects are then used to generate the three RAS signals which are provided to the three banks of memory. A fourth PROM output is supplied to the low power inverter chain to generate the CAS signal. After two gates of delay, this signal is used to control the 74LS157 address multiplexers. These two address multiplexers then take the address bits A0 through A1 and properly time them and multiplex them as seven bits of address to the dynamic memories.

2.3 Memory Array

This schematic contains the 24 memory elements that are used in the memory array. The memory elements utilized in the standard board are NEC 416 dynamic RAMs; however, 4K bit dynamic RAMs can also be utilized with proper strapping.

2.4 Data Bus Buffers

This sheet contains the buffers that are used to separate the data bus into the internal data busses that are required by the disk controller and the memory array. The top two devices are used to separate the data bus into data input and data output for the memory array while the bottom two devices are used to buffer and isolate the system data bus from the disk controller internal bus. The 6306 PROM on the bottom of the schematic is used to control the direction of the data bus buffers. This PROM recognizes when one of the devices on the MDC card must drive onto the system data bus and provides this control signal. Figure 2 identifies the state of the PROM output for the associated input. The five most significant input lines are shown in binary format along the vertical axis. The four least significant address inputs (XXXX on the vertical axis) are identified in hexadecimal notation along the horizontal axis. For each unique address input, the corresponding hex code for the output is found at the crosspoints between the two axes.

2.5 Parallel/Serial Register

This page of the schematic illustrates the parallel/ serial register that is used during both disk READ and WRITE operations. During disk WRITE operations, data from the internal data bus is latched into the register and shifted out on the serial WRITE data line. During READ operations, the decoded data from the data separator is shifted into this register, then read out to the internal data bus and through the data bus buffers, and back to the CPU. The select logic located below the registers is used to control the register shift mode and to provide the proper clocking signals.

2.6 PIO

This portion of the schematic contains the Z80-PIO which is used to latch control data for the disk and to sample status data from the disk. The Z80-CPU bus connects to the PIO and is used for transfer of information between the two. The disk status signals are READY, TRACK 0, SECTOR MARKER, and WRITE PROTECT. These signals are

terminated with 220 ohm and 330 ohm pull-up and pull-down resistors, respectively. The CRC error indicator from the CRC circuit is also provided to the PIO for CPU status checking. The PIO is also used to latch the control information for the disk drive. The control signals, DIRECTION, STEP, and four DISK SELECT lines are provided as outputs with open collector buffering. There are three other control signals that are required by the disk controller that must be separately timed, and the 74LS175 is used for this function. The READ, WRITE, and ENABLE CRC signals are latched by the PIO but are separately timed by the strobe signal from the timing generator to insure proper timing.

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
00000XXXX	08	08	08	08	08	-00-	08	08	08	08	08	08	08	08	08	08
00010XXXX	08	08	08	08	08	08	08	08	08	08	08	08	08	08	08	08
00100XXXX	08	08	08	08	08	-00-	08	08	08	-00-	08	08	08	08	08	08
00110XXXX	08	08	08	08	08	08	08	08	08	-00-	08	08	08	08	08	08
01000XXXX	08	08	08	08	08	-00-	08	08	08	08	08	08	08	08	08	08
01010XXXX	08	08	08	08	08	08	08	08	08	08	08	08	08	08	08	08
01100XXXX	08	08	08	08	08	-00-	08	08	08	08	08	08	08	08	08	08
01110XXXX	08	08	08	08	08	08	08	08	08	08	08	08	08	08	08	08
10000XXXX	08	08	08	08	08	08	08	08	08	08	08	08	08	08	08	08
10010XXXX	08	08	08	08	08	-00-	08	08	08	08	08	08	08	08	08	08
10100XXXX	08	08	08	08	08	08	08	08	08	-00-	08	08	08	08	08	08
10110XXXX	08	08	08	08	08	-00-	08	08	08	-00-	08	08	08	08	08	08
11000XXXX	08	08	08	08	08	08	08	08	08	08	08	08	08	08	08	08
11010XXXX	08	08	08	08	08	-00-	08	08	08	08	08	08	08	08	08	08
11100XXXX	08	08	08	08	08	08	08	08	08	08	08	08	08	08	08	08
11110XXXX	08	08	08	08	08	-00-	08	08	08	08	08	08	08	08	08	08

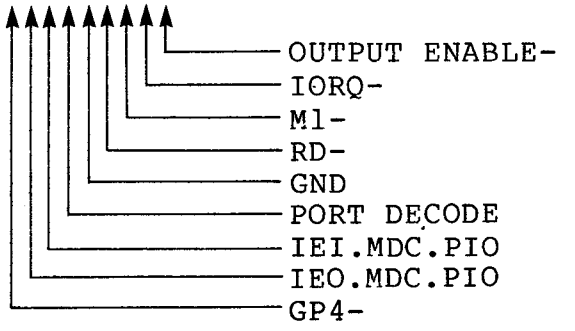


FIGURE 2. MDC Bus Control PROM at Location A54

2.7 Timing Generator and Wait Control Logic

This sheet contains the circuitry that is used to generate the timing pulses that are required during the WRITE operations and also the logic that is used to control the WAIT signal which is used during both READ and WRITE operations. The four counter circuits (74LS161) are used to divide the 8 PHI clock into the proper timing signals. Strapping options are provided for use with double density disk drives and mini-disk drives. The 74LS51 multiplexer is used to select between the timing pulse from the timing chain while in the WRITE mode and the decoder clock from the data separator in READ mode. This clock is then provided as a shift clock to the parallel/serial register. The WAIT logic is centered around a single 74LS74 flip flop. Each time a data read or data write operation from the MCB Board (SG3- and GP7-) occurs, it sets the flip flop which pulls the WAIT- line low and causes the CPU to stop. This WAIT state is then held until such time as the DONE- signal is generated by the timing generator. This signal indicates that the parallel/serial register has been completely filled during READ operations or emptied during WRITE operations, and is ready for a new character. Thus, using this simple technique, the CPU speed is exactly synchronized to the disk operating speed.

2.8 CRC and Data Separator

This schematic includes the CRC circuit which is used during both READ and WRITE operations. During WRITE operations, the data that is being written onto the disk is also clocked into this circuit. This data is then used to generate a 16-bit CRC word which is to be appended to the end of the WRITE data. Multiplexer logic provided by the 74LS51 circuit selects between the actual SERIAL WRITE DATA and the CRC chip output. This circuit is also used during READ operations. During these operations, the READ DATA is clocked into the CRC chip so that at the end of every block of READ DATA, the generated CRC word can be compared with the CRC word that is received from the disk drive. If an error occurs, the CRC circuit will generate the CRC error flag which can be read into the CPU via the PIO. The ENABLE CRC signal which is used by the multiplexer during WRITE operations is provided by the CPU via the PIO. Below this is the data separator. This circuit functions by separating the clock and the data from the disk drive into a data signal and a clock signal which will then be provided to the serial/parallel register.

This circuit also contains a start bit detector which looks for the first logic 1 written after the READ mode is enabled. This start bit detector is used for formatting disks as described in Section 3.0.

SECTION 3. DISK DATA FORMATTING

3.1 Introduction

All formatting of the data onto the disk is accomplished under the control of the Z80-CPU on the MCB board. Thus, this disk contoller can operate with a variety of floppy disk drive configurations. However, as an option, Zilog offers PROM-based software which can be be used to control up to eight Shugart 800 Floppy Disk drives. This software assumes that 32 hard sectors are utilized per track and 77 tracks are utilized per disk. The software provides all control functions for the disk and does all data transfer.

3.2 Sector Data Format

All formatting of the data on the disk is accomplished under the control of the CPU. Figure 3-1 represents the formatting structure: 16 bytes of all zeroes for the preamble; one byte for sector address with the first bit being a start bit; one byte for the track address; then 128 bytes of data; 4 bytes of linkage (forward/backward) for file maintenance; two bytes of CRC; and then a postamble of all zeroes.

In this format, the user may record up to 32 sectors (records) per track. Each track is started by a physical index pulse, and each sector is started by a physical sector pulse. This type of recording is called hard sectoring.

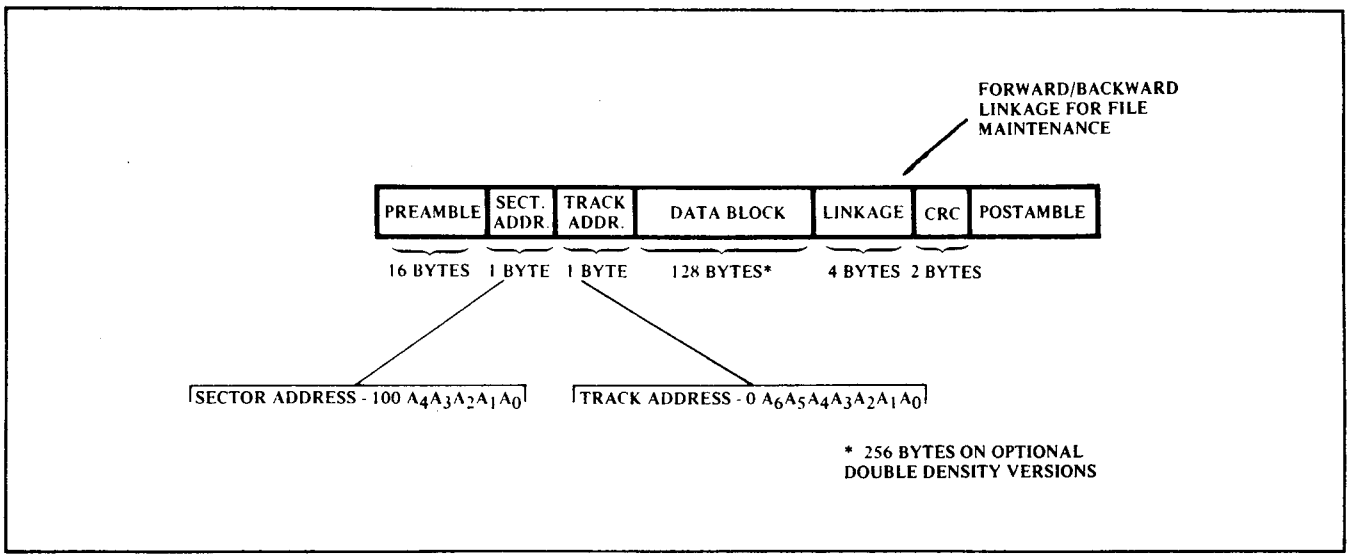


Figure 3-1
DISK FORMAT

BIT CELL: As shown in Figure 3-2, the clock bits and data bits (if present) are interleaved. By definition, a bit cell is the period between the leading edge of one clock bit and the leading edge of the next clock bit.

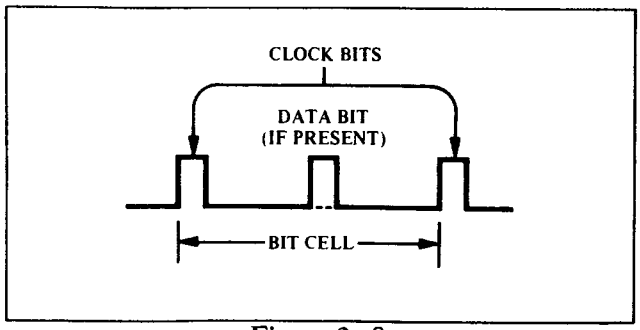


Figure 3-2
BIT CELL

BYTE: A byte, when referring to serial data (being written onto or read from the disk drive) is defined as eight consecutive bit cells. The least significant bit cell is defined as bit cell 0 and the most significant bit cell is defined as bit cell 7. When reference is made to a specific data bit (i.e.,data bit 3), it is with respecct to the corresponding bit cell (bit cell 3).

During the write operation, bit cell 7 of each byte is transferred to the disk drive first with bit cell 0 being transferred last.

When data is read back from the drive, bit cell 7 of each byte will be transferred first with bit cell 0 last. As with writing, the most significant byte will be transferred first from the drive to the user.

3.3 Recording Format

Data is written on the diskette using frequency modulation as the recording mode; i.e., each data bit recorded on the diskette has an associated clock bit recorded with it. This is referred to as FM. Data written on and read back from the diskette takes the form as shown in Figure 3-3. The binary data pattern shown represents a 101.

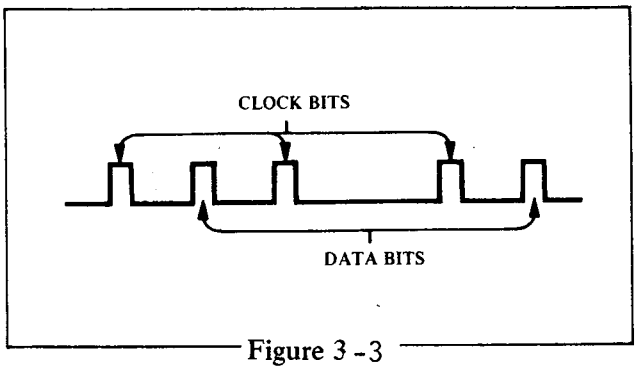


Figure 3-3
DATA PATTERN

Figure 3 - 4 illustrates the relationship of the bits with a byte, and Figure 3 - 5 illustrates the relationship of the bytes for READ and WRITE data.

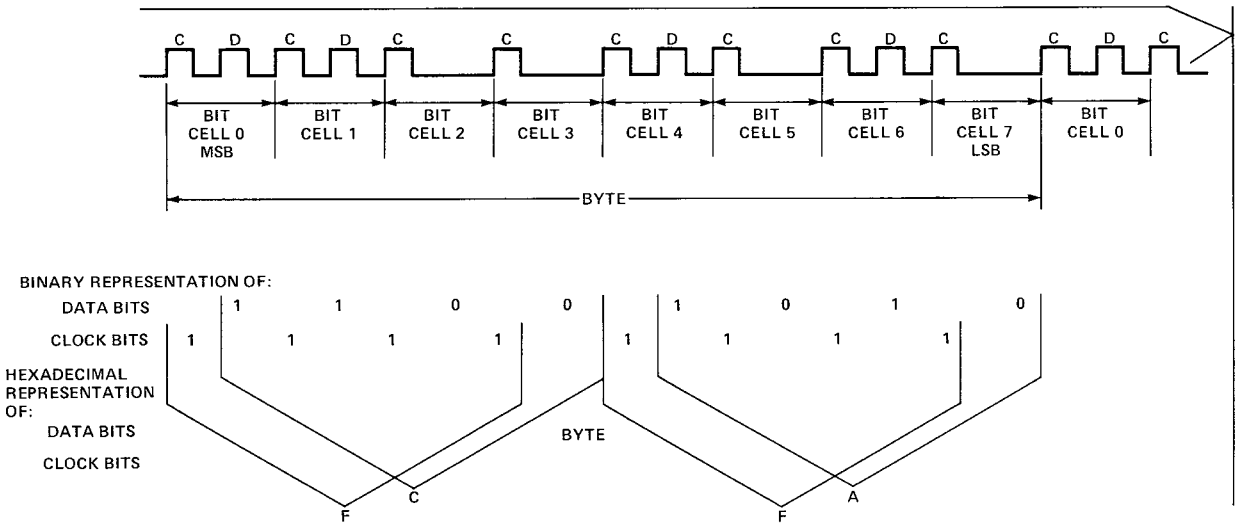


Figure 3 - 4
BITS WITHIN A BYTE

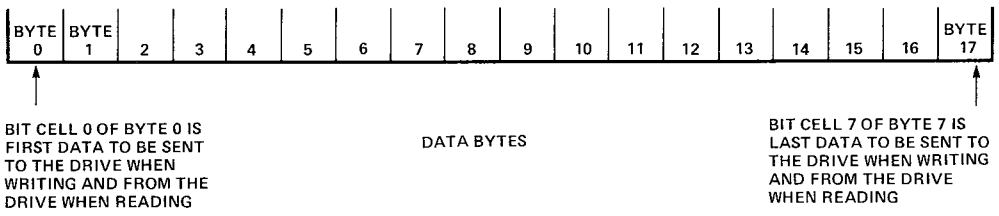


Figure 3 - 5
DATA BYTE RELATIONSHIPS

SECTION 4. MDC MEMORY ADDRESS PROGRAMMING

4.1 Introduction

The addresses associated with the memories on the MDC are programmed by a combination of a jumper wire plug and a 32 x 8 bit bipolar PROM. The jumper wires are used to program the address multiplexer for either 4K or 16K dynamic RAMs. The PROM is used to define which 4K page of memory will respond to a given memory address. This scheme allows a wide range of memory configurations to be implemented very easily.

As shown in Sheet 2 of the MDC logic diagram, inputs and outputs of the memory address PROM (A3) are defined as follows:

INPUTS
- A0 = Address bit 12
- A1 = Address bit 13
- A2 = Address bit 14
- A3 = Address bit 15
- A4 = RFSH- (memory refresh signal from CPU)

OUTPUTS

O1 = Not used	O5 = CAS-
O2 = Not used	O6 = RAS0-
O3 = Not used	O7 = RAS1-
O4 = Not used	O8 = RAS2-

The PROM is enabled only when MREQ- is low to prevent output spiking. The PROM is programmed to output a zero on all RAS lines when RFSH- is low and to output a zero on CAS- and the appropriate RAS- line when address bits 12 through 15 are addrressing a 4K memory block on the MDC.

4.2 Programming for 4K RAMs

Wiring for the 4K jumper plug is listed below:

FROM	TO	
J1-10	J1-11, J1-12	(GND)
J1-13	J1-15	(AB0)
J1-14	J1-16	(AB6)

The following table shows the standard programming of A3 for use with 4K RAMs.

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
00	1F	1F	1F	1F	1F	1F	1F	1F	1F	1F	1F	1F	1F	1F	1F	1F
10	FF	FF	CF	AF	6F	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF

This programming places the RAMs in the address space 2000H to 4FFFH.

4.3 Programming for 16K RAMs

Wiring for the 16K jumper plug is listed below:

FROM	J1-13	TO	J1-15	(AB0)
	J1-1		J1-14	(AB12)
	J1-11		J1-16	(AB6)
	J1-2		J1-12	(AB13)

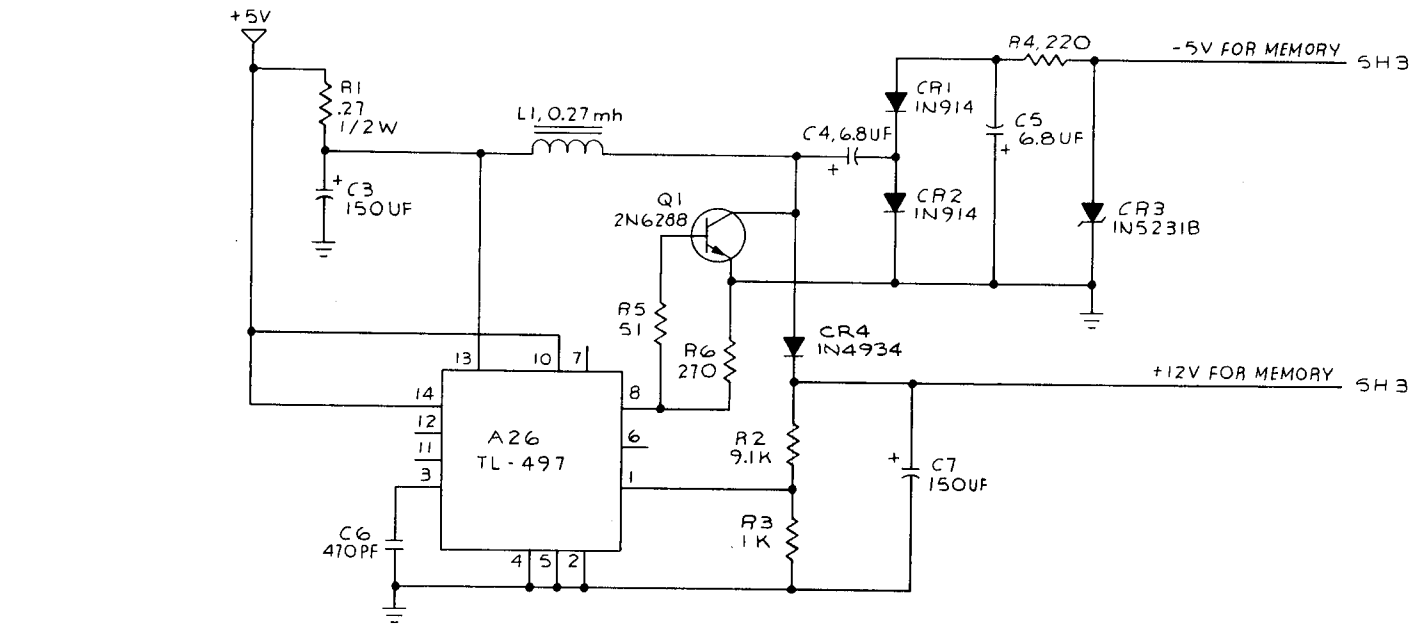
The table below shows the standard programming of A3 for use with 16K RAMs.

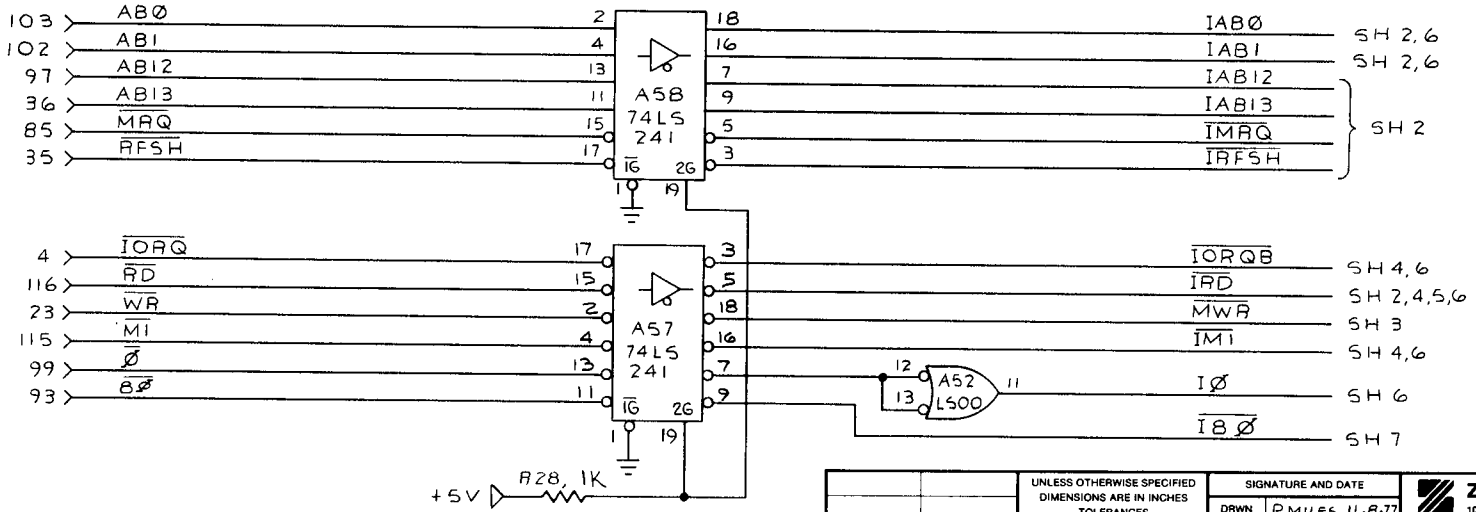
	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
00	1F	1F	1F	1F	1F	1F	1F	1F	1F	1F	1F	1F	1F	1F	1F	1F
10	FF	CF	CF	CF	FF	FF	FF	FF	CF	AF	AF	AF	AF	6F	6F	6F

This programming places the MDC RAM in the memory spaces 1000 to 4000H and 8000H to FFFFH.

5.0 SCHEMATICS (MDC)

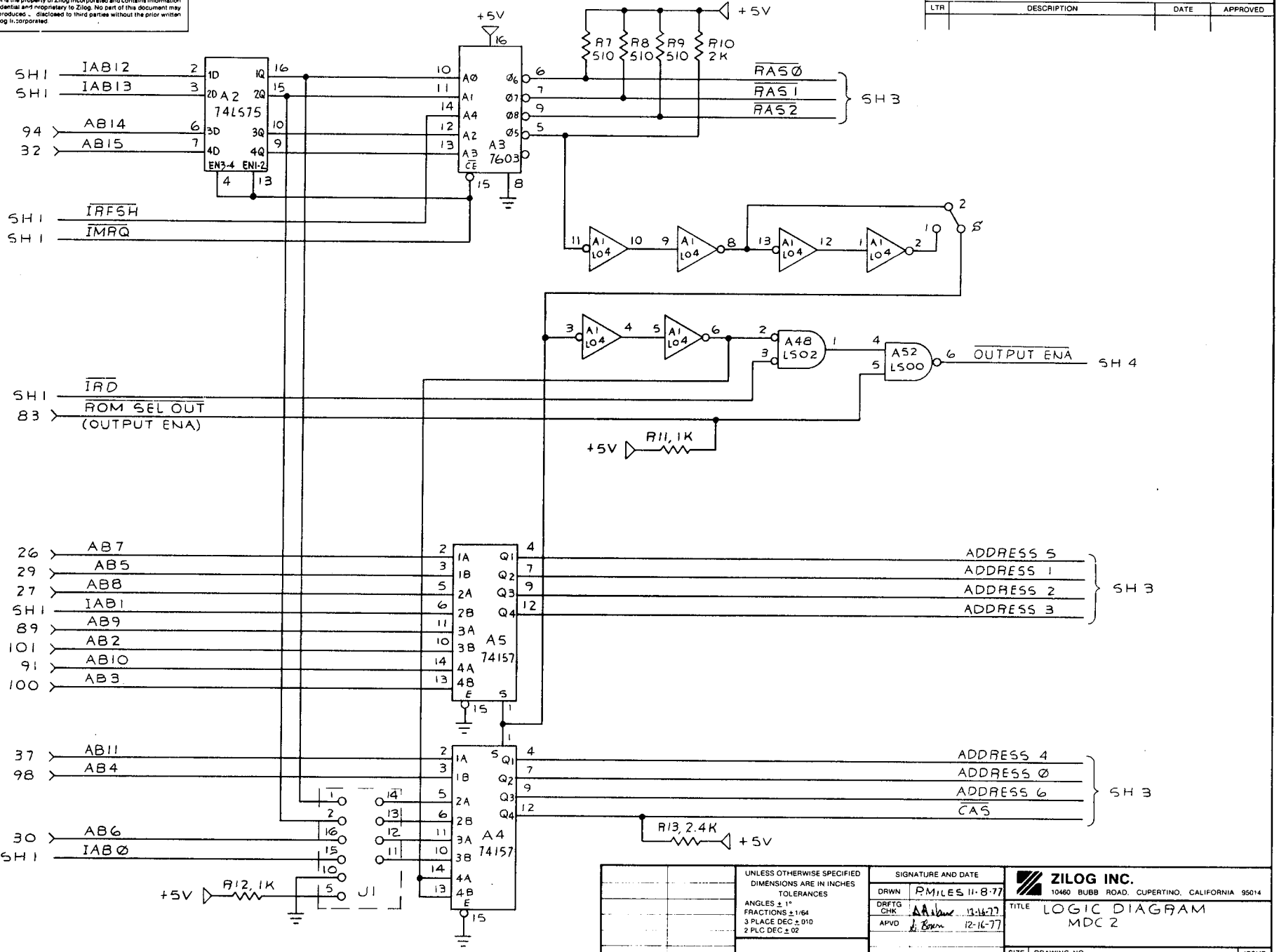
REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
A	RELEASE ECN 00172	12-16-77	DRB 12-16-77





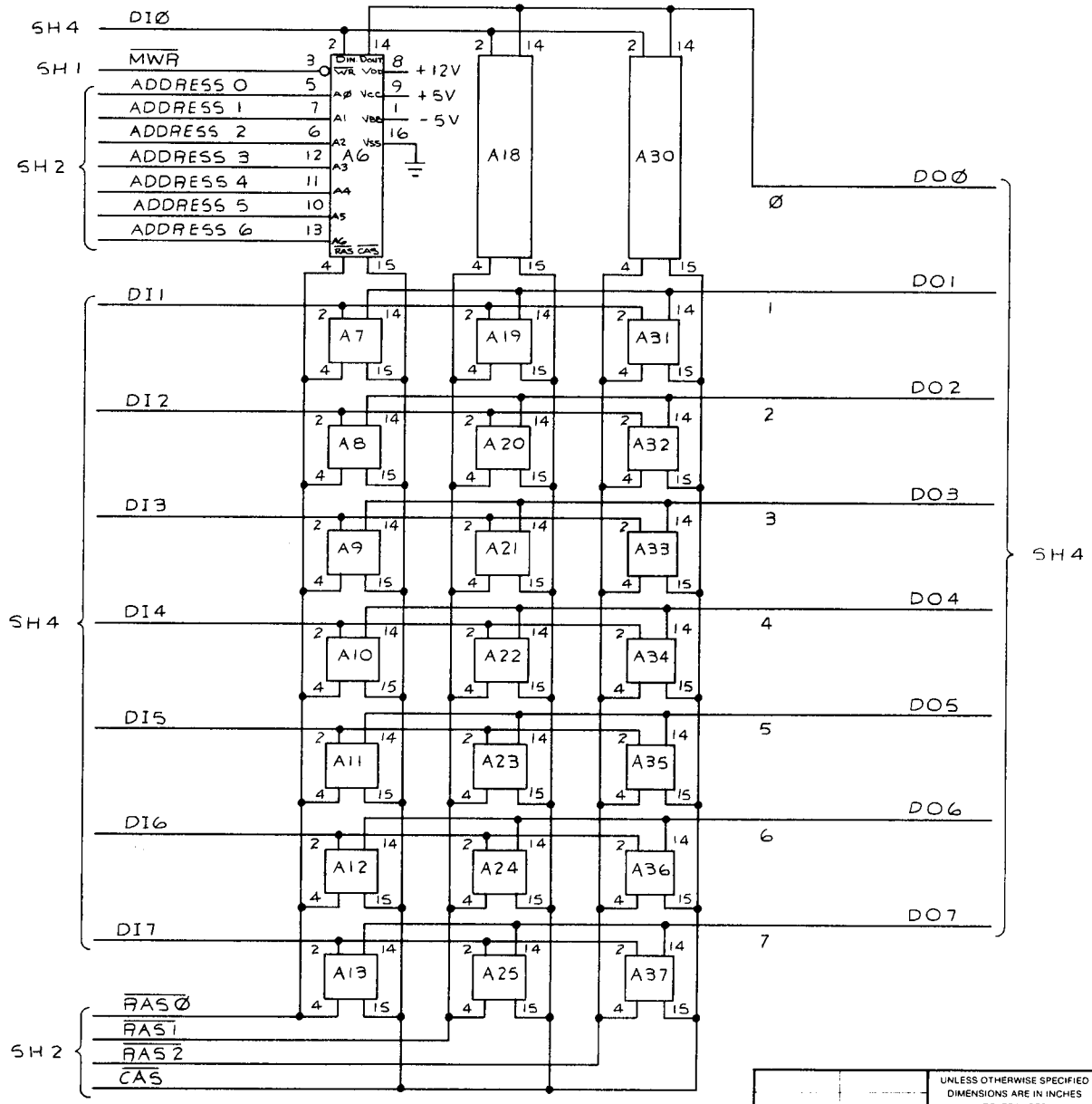
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ANGLES ± 1° FRACTIONS ± 1/64 3 PLACE DEC ± 010 2 PLC DEC ± 02	SIGNATURE AND DATE	ZILOG INC. 10460 BUBB ROAD, CUPERTINO, CALIFORNIA 95014	
	DRWN R MILES 11-8-77	TITLE LOGIC DIAGRAM MDC2	
	DRFTG CHK 12-16-77		
	APVD 12-16-77		
NEXT ASSY / USED ON	MAT'L:	FINISH	SIZE C / DRAWING NO. DZ-0015-04 / ISSUE A
APPLICATION			SCALE NONE / SHEET 1 OF 8

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED



UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ANGLES ± 1° FRACTIONS ± 1/64 3 PLACE DEC ± .010 2 PLC DEC ± .02	SIGNATURE AND DATE	ZILOG INC. 10460 BUBB ROAD, CUPERTINO, CALIFORNIA 95014	
	DRWN R MILES 11-8-77	TITLE LOGIC DIAGRAM MDC 2	
	DRFTG CHK 13-16-77		
	APVD 12-16-77		
NEXT ASSY / USED ON / APPLICATION	MAT'L	FINISH	SIZE C / DRAWING NO DZ-0015-04 / ISSUE A
			SCALE — / SHEET 2 OF 8

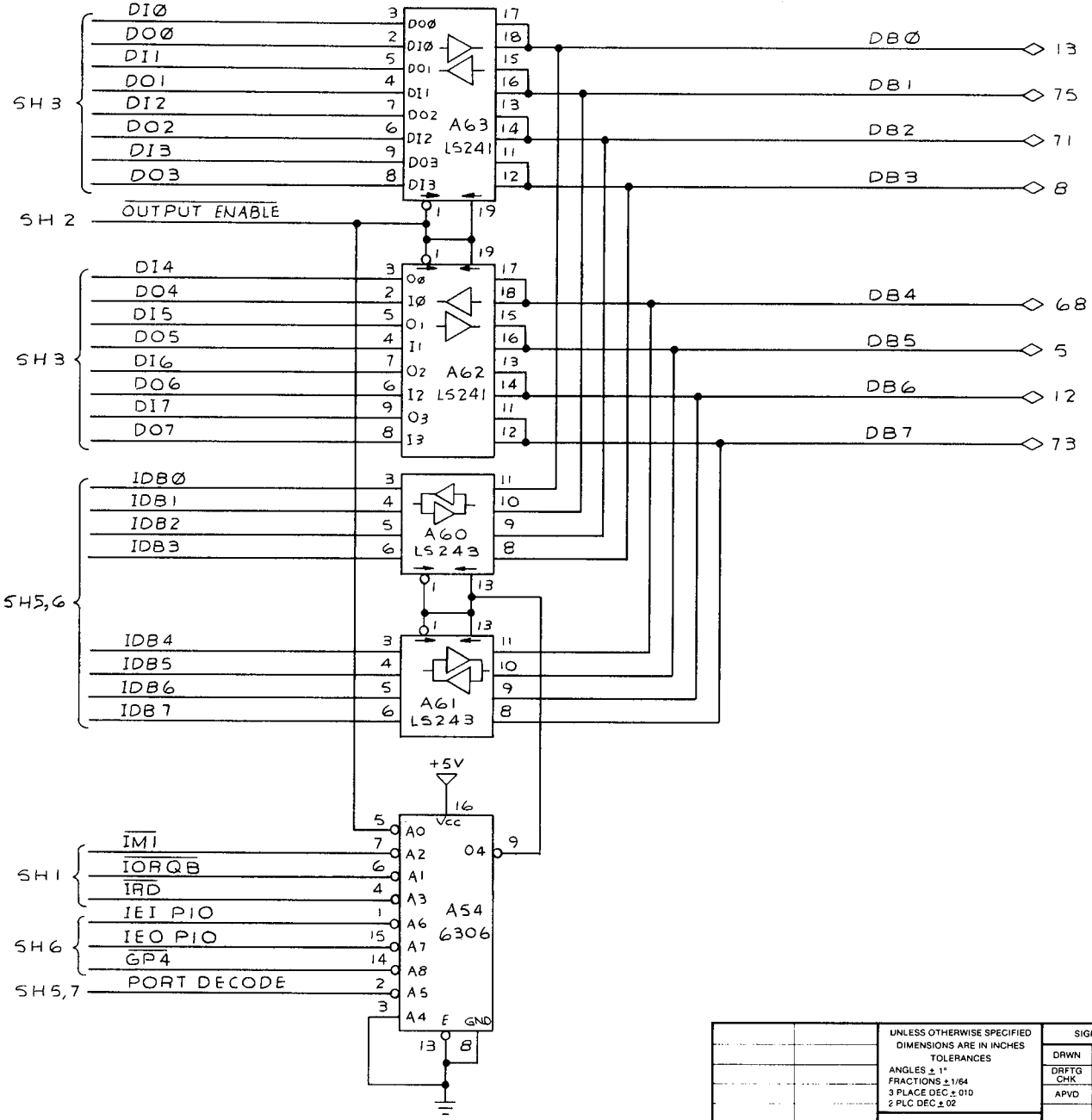
REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED



NOTES:
1. ALL DEVICES ARE WIRED TYP. TO A6.

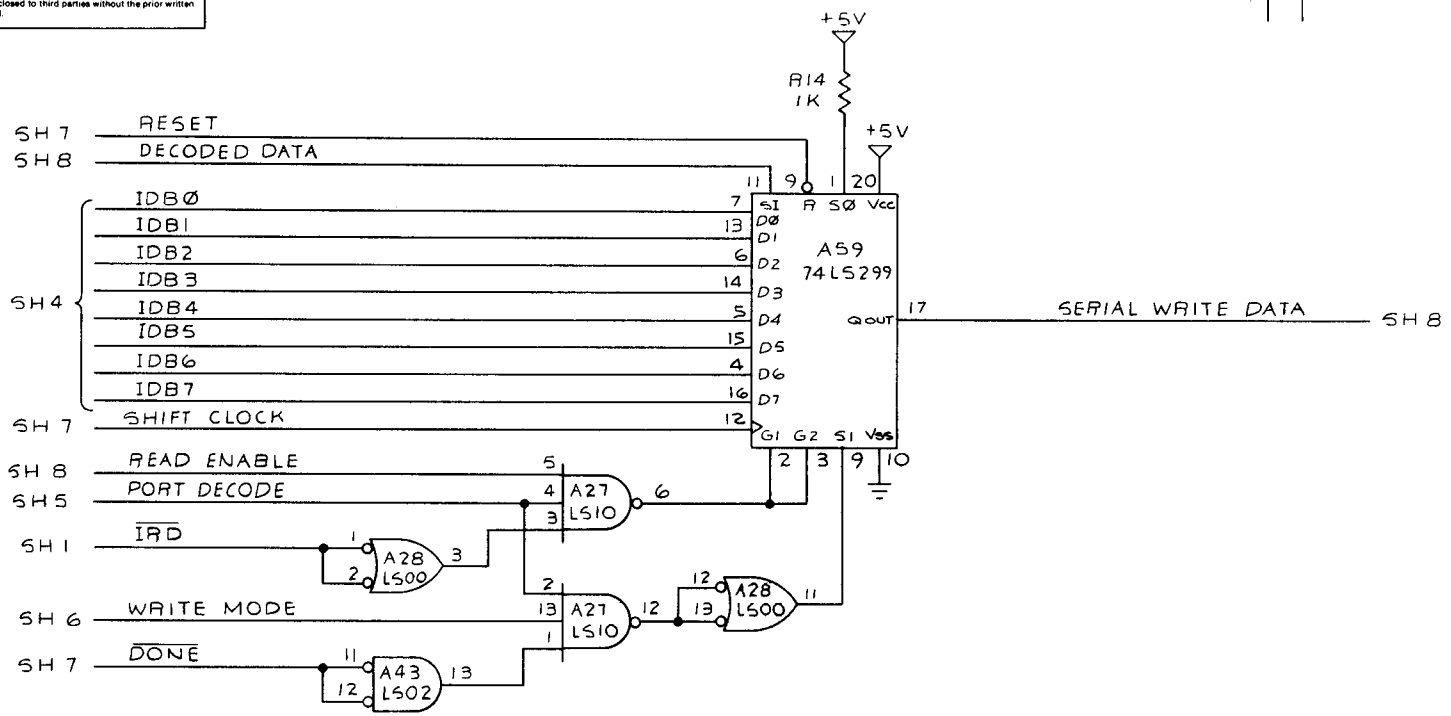
	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ANGLES ± 1° FRACTIONS ± 1/64 3 PLACE DEC ± .010 2 PLC DEC ± .02	SIGNATURE AND DATE	ZILOG INC. 10460 BUBB ROAD CUPERTINO, CALIFORNIA 95014		
		DRAWN P MILES 11-8-77	TITLE LOGIC DIAGRAM MDC 2		
		DRFTG CHK 12-16-77			
		APVD 12-16-77			
NEXT ASSY USED ON	MAT'L	FINISH	SIZE C	DRAWING NO 02-0015-04	ISSUE A
APPLICATION			SCALE	SHEET 3 OF 8	

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED

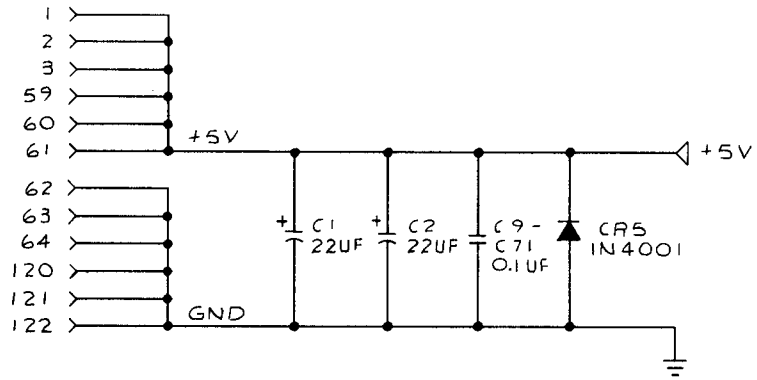


	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ANGLES ± 1° FRACTIONS ± 1/64 3 PLACE DEC ± 010 2 PLC DEC ± 02	SIGNATURE AND DATE	ZILOG INC. 10460 BUBB ROAD, CUPERTINO, CALIFORNIA 95014
		DRWN P. MILES	TITLE LOGIC DIAGRAM MDC 2
		DRFTG CHK 12-16-77	
		APVD 12-16-77	
NEXT ASSY / USED ON	MAT'L:	FINISH	SIZE C / DRAWING NO DZ-0015-C4 / ISSUE A
APPLICATION			SCALE — / SHEET 4 OF 8

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED

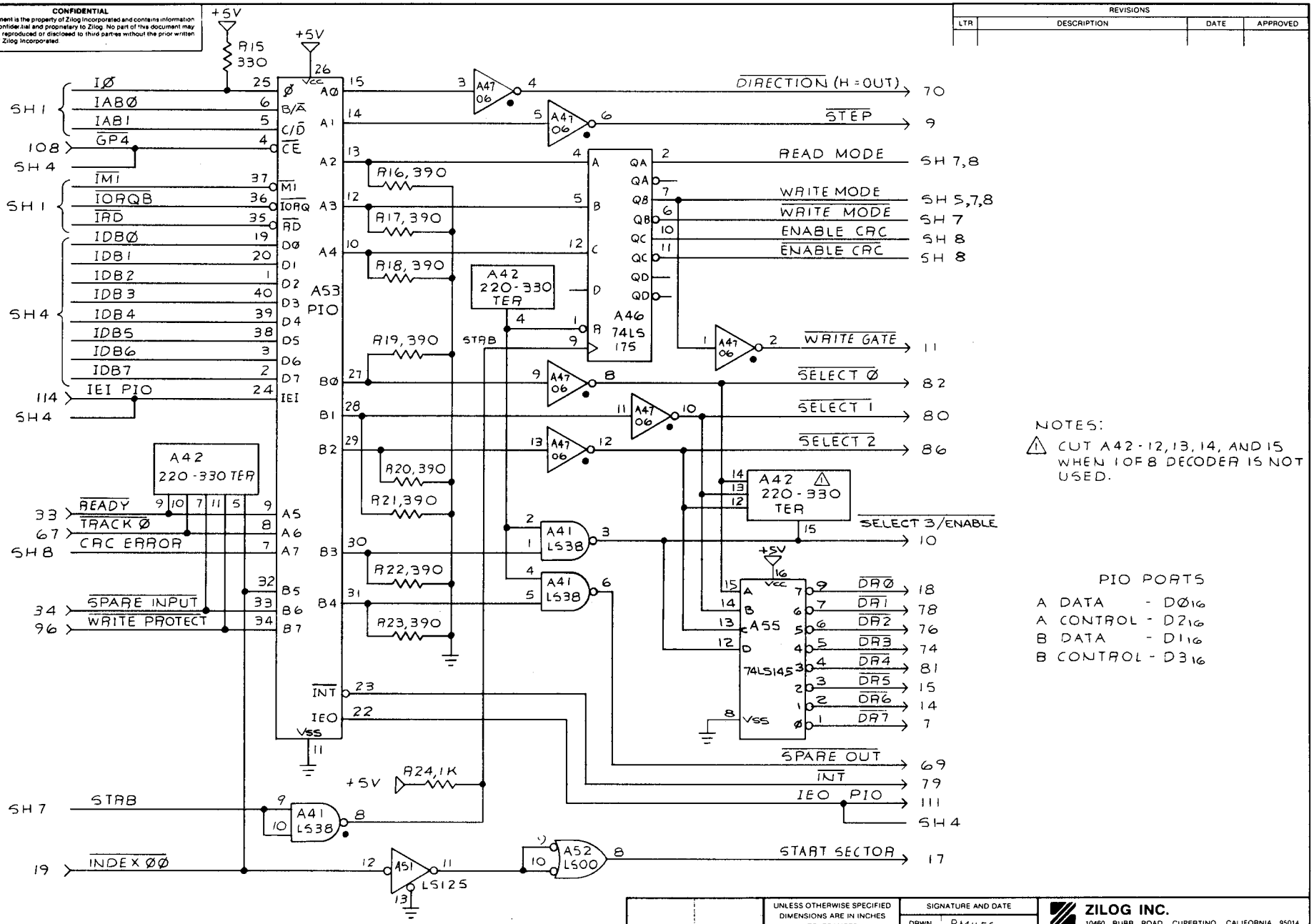


DISK DATA PORT = CF16



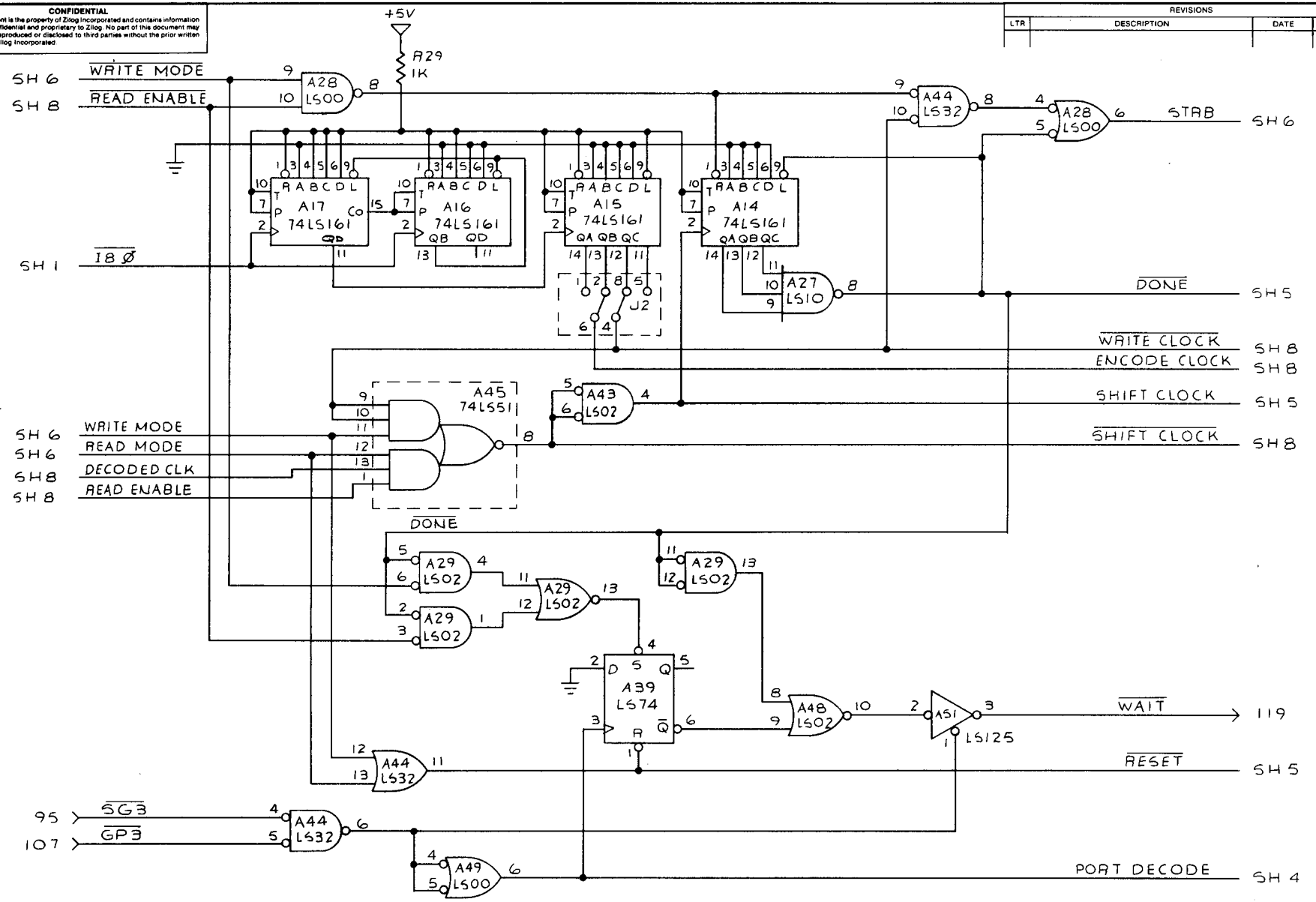
		UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ANGLES ± 1° FRACTIONS ± 1/64 3 PLACE DEC ± .010 2 PLC DEC ± .02	SIGNATURE AND DATE	ZILOG INC. 10460 BUBB ROAD. CUPERTINO. CALIFORNIA 95014	
			DRWN P MILES	TITLE LOGIC DIAGRAM MDC 2	
			DRFTG CHK 12-11-77		
			APVD D Brown 12-16-77		
NEXT ASSY	USED ON	MAT'L	FINISH	SIZE C	DRAWING NO. DZ-0015-04 ISSUE A
APPLICATION				SCALE	SHEET 5 OF 8

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED



	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ANGLES ± 1° FRACTIONS ± 1/64 3 PLACE DEC ± .010 2 PLC DEC ± .02	SIGNATURE AND DATE DRWN P.MILES DRFTG CHK 12-16-77 APVD 12-16-77	ZILOG INC. 10460 BUBB ROAD, CUPERTINO, CALIFORNIA 95014
NEXT ASSY / USED ON	MAT'L	FINISH	TITLE LOGIC DIAGRAM MDC 2
APPLICATION			SIZE C DRAWING NO DZ-0015-04 ISSUE A
			SCALE — SHEET 6 OF 8

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED



8 Ø = 19.6608 MHZ	
DATA RATE = 517.3 KBS	1-6,2-4
DATA RATE = 258.7 KBS	2-6,8-4
DATA RATE = 129.3 KBS	8-6,5-4

NOTE: FOR RATES OTHER THAN 258.7 KBS THE A C OF THE DATA SEPARATOR (SHT 8) MUST BE CHANGED

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES
ANGLES ± 1°
FRACTIONS ± 1/64
3 PLACE DEC ± .010
2 PLC DEC ± .02

SIGNATURE AND DATE		
DRWN	P. MILES	
DRFTG CHK		12-16-77
APVD	J. Brown	12-16-77

NEXT ASSY | USED ON
APPLICATION
MAT'L
FINISH

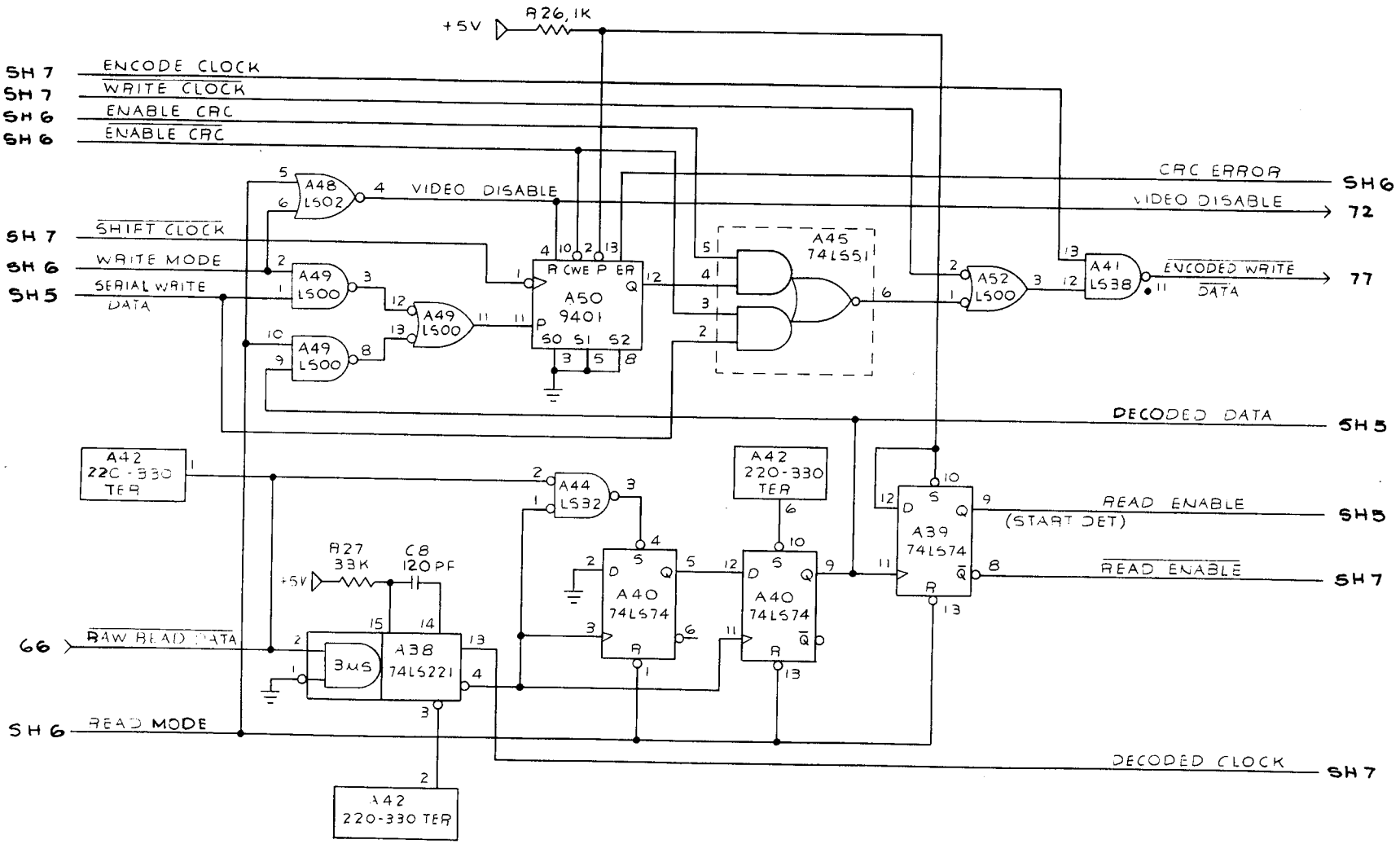
ZILOG INC.
10460 BUBB ROAD, CUPERTINO, CALIFORNIA 95014

TITLE LOGIC DIAGRAM MDC2

SIZE C | DRAWING NO DZ-0015-04 | ISSUE A

SCALE ——— | SHEET 7 OF 8

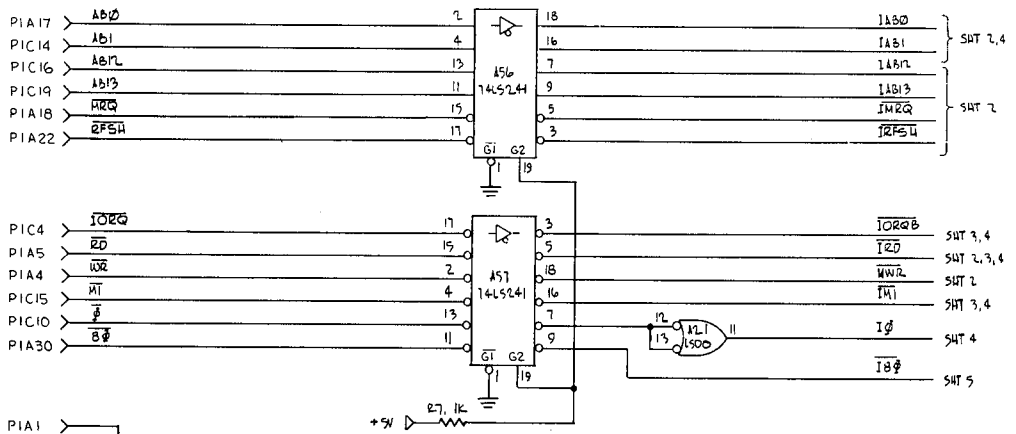
REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED

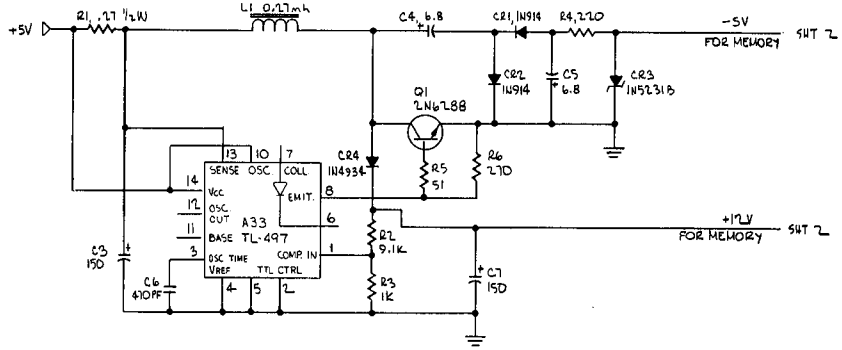


	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ANGLES ± 1° FRACTIONS ± 1/64 3 PLACE DEC ± .010 2 PLC DEC ± .02	SIGNATURE AND DATE DRWN AMILES DRFTG CHK 12-16-77 APVD A. Brown 12-16-77	ZILOG INC. 10460 BUBB ROAD, CUPERTINO, CALIFORNIA 95014	
NEXT ASSY / USED ON / APPLICATION	MAT'L:	FINISH	TITLE LOGIC DIAGRAM MDC 2	
			SIZE C / DRAWING NO. DZ-0015-04 / ISSUE B	
			SCALE — / SHEET 8 OF 8	

5.0 SCHEMATICS (MDC/E)

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
A	ECN 00279	3-78	AL





NOTES:

1. UNLESS OTHER SPECIFIED:
   RESISTORS ARE CARBON, ¼W, 5%.
   CAPACITORS ARE IN MICROFARADS.

(2) A10-A16, A25-A32, A40-A47 TO BE WIRED TYP TO A9.

(3) PIO PORTS
- A DATA - $D0_{16}$
- A CONTROL - $D2_{16}$
- B DATA - $D2_{16}$
- B CONTROL - $D3_{16}$

(4)

8φ = 19.6608 MHz	
DATA RATE = 511.3 KBS	1-6, 2-4
DATA RATE = 258.7 KBS	2-6, 8-4
DATA RATE = 129.3 KBS	8-6, 5-4
FOR RATES OTHER THAN 258.7 KBS THE RC OF THE DATA SEPARATOR (SHT6) MUST BE CHANGED	

(5) DISK DATA PORT = CF_{16}

ITEM	QTY	TYPE	ZILOG PART NO	DESCRIPTION	REF. DES

PARTS LIST

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES
ANGLES ± 1°
FRACTIONS ± 1/64
2 PLACE DEC ± .010
3 PLC DEC ± .02

SIGNATURE AND DATE	
DRAWN	1-18-78
DRFTG CHK	
APVD	1-18-78

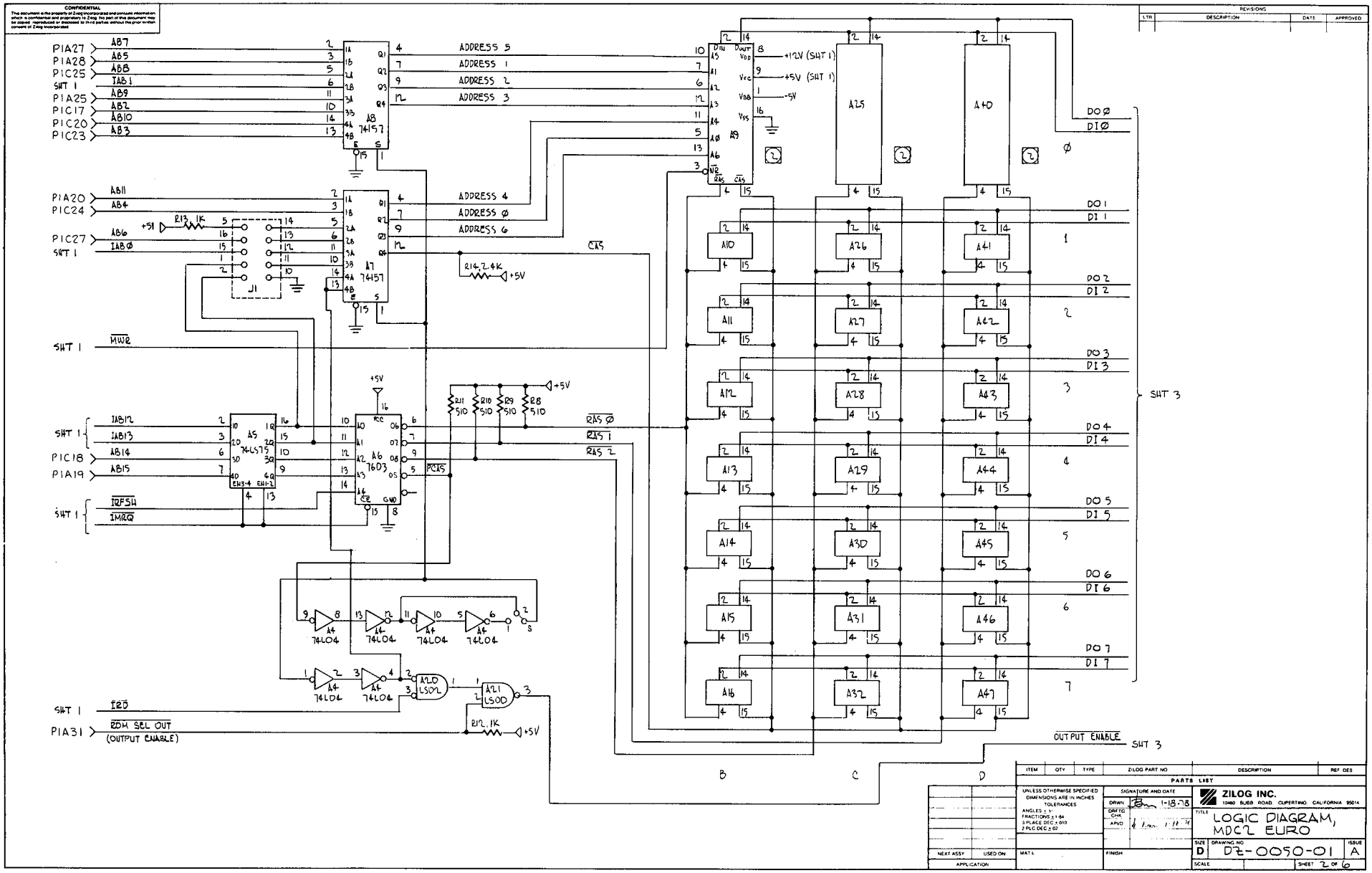
ZILOG INC.
10460 BUBB ROAD CUPERTINO, CALIFORNIA 95014

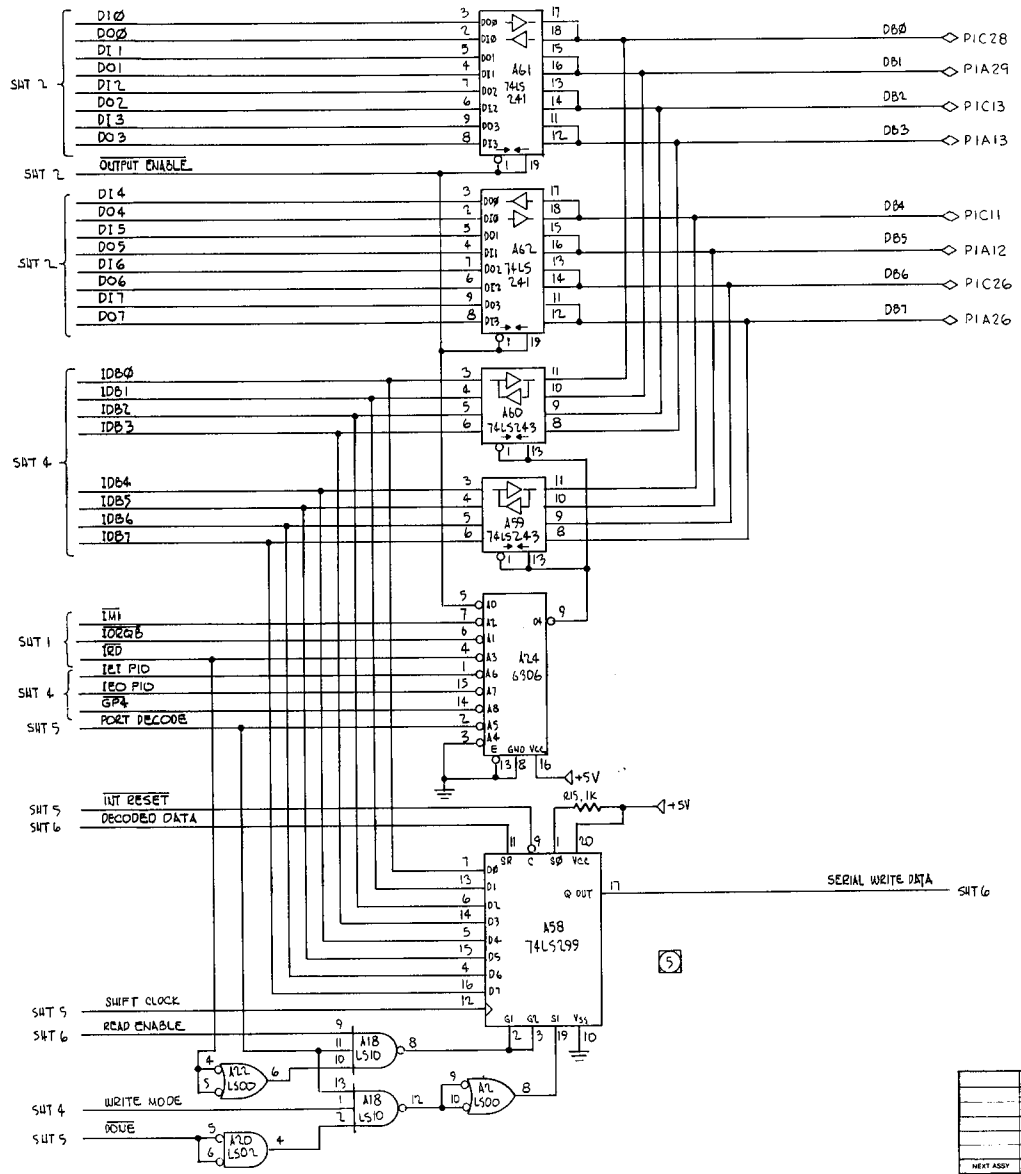
TITLE: LOGIC DIAGRAM, MDC2 EURO

SIZE	DRAWING NO	ISSUE
D	D2-0050-01	A

SCALE | SHEET 1 OF 6

NEXT ASSY | USED ON | APPLICATION | MAT'L | FINISH


CONFIDENTIAL
REVISIONS
LTR DESCRIPTION DATE APPROVED
PIA27 AB7
PIA28 AB5
PIC25 AB8
SHT 1 IAB1
PIA25 AB9
PIC17 AB12
PIC20 AB10
PIC23 AB13
ADDRESS 5
ADDRESS 1
ADDRESS 2
ADDRESS 3
PIA20 AB11
PIC24 AB4
PIC27 AB6
SHT 1 IABØ
ADDRESS 4
ADDRESS Ø
ADDRESS 6
R13 1K
+5V
R14 2.4K
CAS
J1
SHT 1 MWR
SHT 1 IAB12
IAB13
PIC18 AB14
PIA19 AB15
SHT 1 IRFSH
IMRQ
R11 510
R10 510
R9 510
R8 510
RAS Ø
RAS 1
RAS 2
PCAS
SHT 1 IRD
PIA31 RDM SEL OUT
(OUTPUT ENABLE)
R12 1K
+12V (SHT 1)
+5V (SHT 1)
-5V
DO Ø
DI Ø
DO 1
DI 1
DO 2
DI 2
DO 3
DI 3
DO 4
DI 4
DO 5
DI 5
DO 6
DI 6
DO 7
DI 7
SHT 3
OUTPUT ENABLE
SHT 3
B
C
D
ITEM QTY TYPE ZILOG PART NO DESCRIPTION REF DES
PARTS LIST
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES
ANGLES ± 1°
FRACTIONS ± 1/64
3 PLACE DEC ± .010
2 PLC DEC ± .02
SIGNATURE AND DATE
DRAWN 1-18-78
DRFTG CHK
APVD
NEXT ASSY USED ON
APPLICATION
MATL
FINISH
ZILOG INC.
10460 BUBB ROAD CUPERTINO CALIFORNIA 95014
TITLE LOGIC DIAGRAM, MDC2 EURO
SIZE D DRAWING NO D2-0050-01 ISSUE A
SCALE SHEET 2 OF 6



REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED

ITEM	QTY	TYPE	ZILOG PART NO	DESCRIPTION	REF DES

PARTS LIST

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES
ANGLES ± 1°
FRACTIONS ± 1/64
3 PLACE DEC ± 010
2 PLC DEC ± 03

NEXT ASSY | USED ON
APPLICATION

MAT'L

FINISH

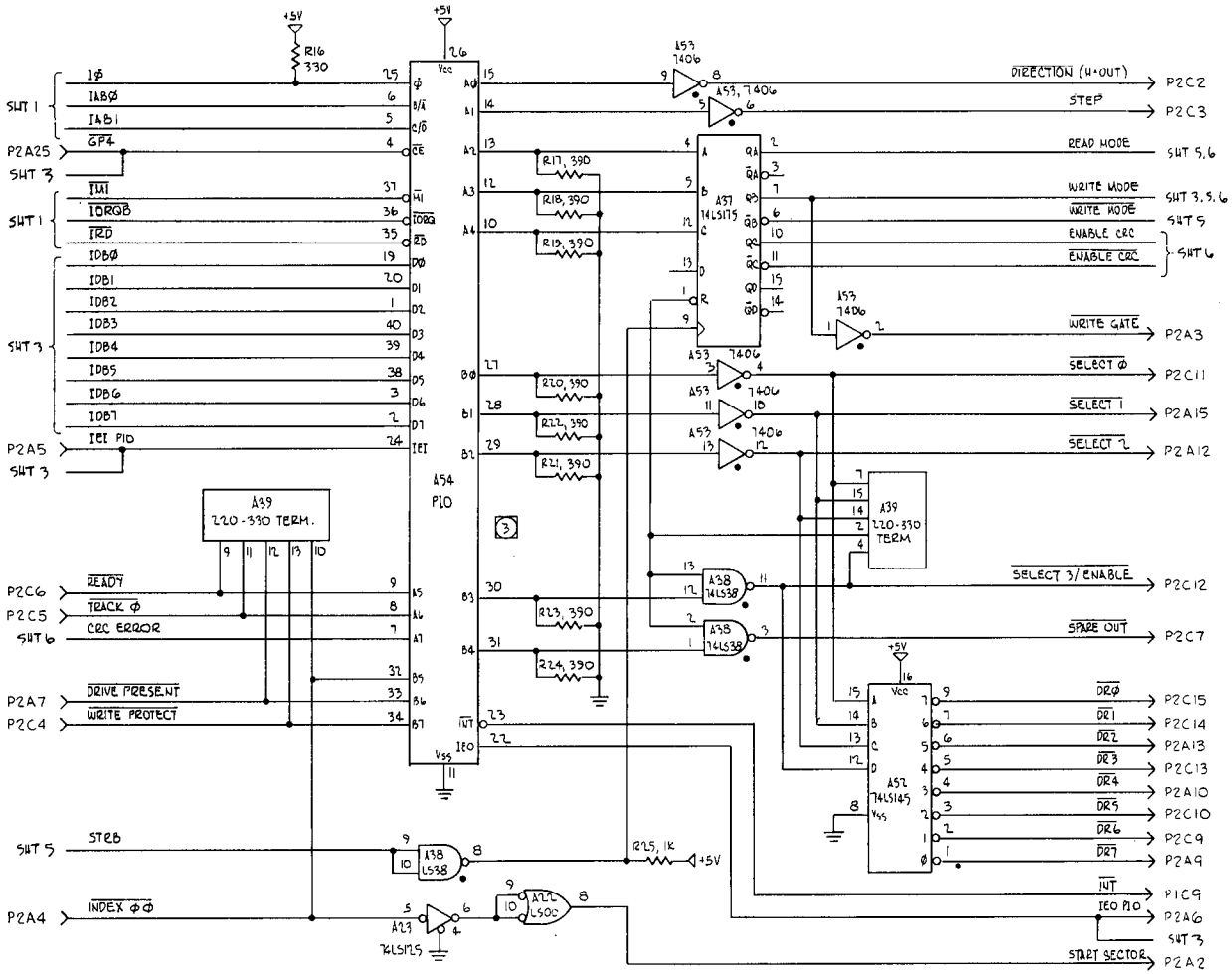
SIGNATURE AND DATE
DRAWN 1-18-78
DRFTG CHK
APVD 1-18-78

ZILOG INC.
10460 BUBB ROAD, CUPERTINO, CALIFORNIA 95014

TITLE: LOGIC DIAGRAM, MDC2 EURO

SIZE D | DRAWING NO D2-0050-01 | ISSUE A

SCALE | SHEET 3 OF 6



ITEM	QTY	TYPE	ZILOG PART NO	DESCRIPTION	REF DES

PARTS LIST

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES
ANGLES ± 1°
FRACTIONS ± 1/64
2 PLACE DEC ± .010
3 PLC DEC ± .02

SIGNATURE AND DATE
DRWN 1-18-82
DSGD CHK
APVD

NEXT ASSY | USED ON
APPLICATION
MAT'L
FINISH

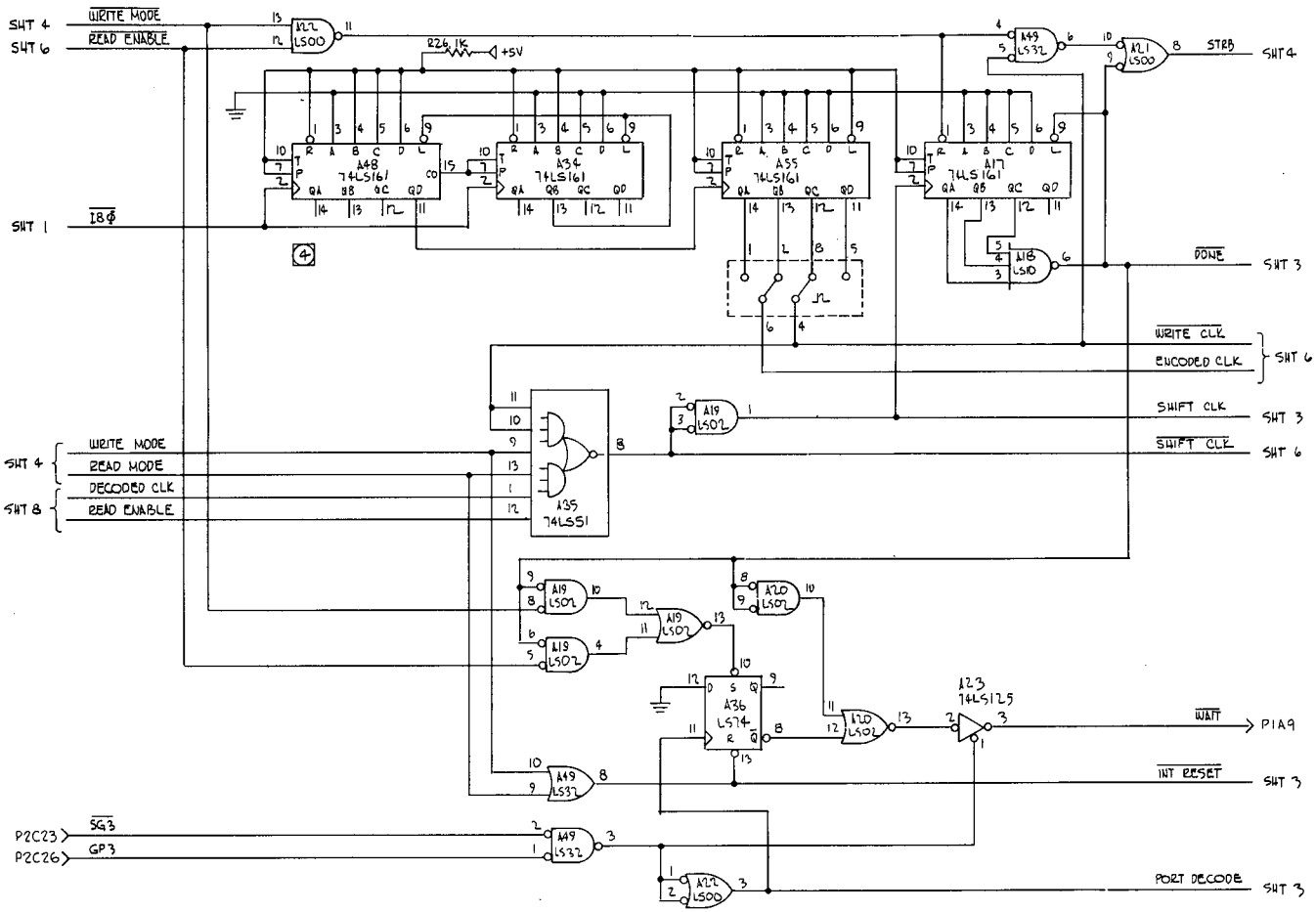
ZILOG INC.
10460 BUBB ROAD CUPERTINO CALIFORNIA 95014

TITLE: LOGIC DIAGRAM, MDC2 EURO

SIZE D | DRAWING NO D7-0050-01 | ISSUE A

SCALE | SHEET 4 OF 6

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED



ITEM	QTY	TYPE	ZILOG PART NO	DESCRIPTION	REF DES

PARTS LIST

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES
ANGLES ± 1°
FRACTIONS ± 1/64
2 PLACE DEC ± .010
3 PLC DEC ± .02

SIGNATURE AND DATE
DRWN Tom 1-18-78
CHK
APVD

NEXT ASSY | USED ON
APPLICATION
MAT'L
FINISH

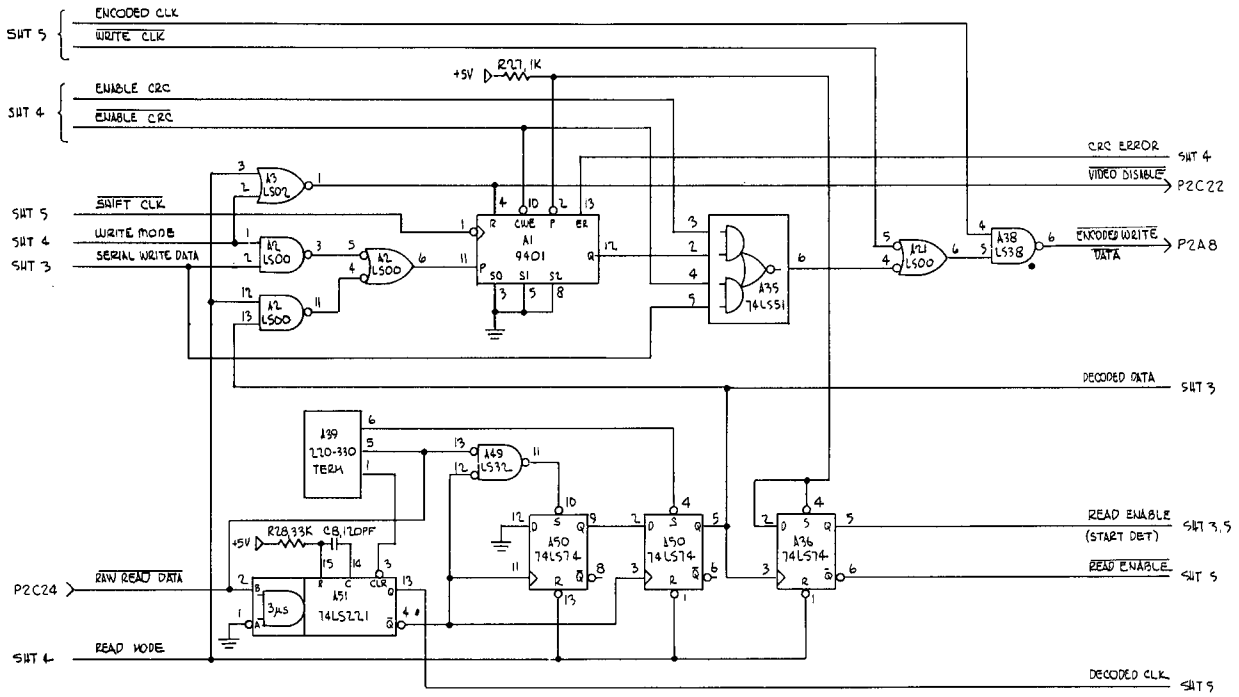
ZILOG INC.
10460 BUBB ROAD CUPERTINO CALIFORNIA 95014

TITLE LOGIC DIAGRAM, MDC2 EURO

SIZE D | DRAWING NO 72-0050-01 | ISSUE A

SCALE | SHEET 5 OF 6

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED



ITEM	QTY	TYPE	ZILOG PART NO	DESCRIPTION	REF DES

PARTS LIST

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES
ANGLES ± 1°
FRACTIONS ± 1/64
3 PLACE DEC ± .010
2 PLC DEC ± .02

SIGNATURE AND DATE
DRAWN 1-18-78
CHK
APVD 1-18-78

ZILOG INC.
10460 BUBB ROAD CUPERTINO CALIFORNIA 95014

TITLE LOGIC DIAGRAM, MDC2 EURO

SIZE D | DRAWING NO. DZ-0050-01 | ISSUE A

SCALE | SHEET 6 OF 6

NEXT ASSY | USED ON | APPLICATION | MAT'L | FINISH

MDC PIN #	SIGNAL NAME	FUNCTION
1	+5V	VCC SUPPLY
2	+5V	
3	+5V	
4	IORQ-	
5	DB5	
6	.	
7	DR7-.(RADIAL SELECT 7-)	
8	DB3	
9	STEP-	
10	SELECT.3-.(BINARY SELECT :	ENABLE-)
11	WRITE.GATE-	
12	DB6	
13	DB0	
14	DR6-.(RADIAL SELECT 6-)	
15	DR5-.(RADIAL SELECT 5-)	
16	.	
17	DISK.(C/T.0)	COMPOSITE SECTOR AND INDEX MARKS
18	DR0-.(RADIAL SELECT 0-)	SYSTEM DISK RADIAL SELECT LINE
19	INDEX00-	SIGNAL TO MCB CTC FOR SECTOR TIMING
20	.	
21	.	
22	.	
23	WR-	
24	.	
25	.	
26	AB7	
27	AB8	
28	.	
29	AB5	
30	AB6	
31	.	
32	AB15	
33	READY-	INDICATES INDEX MARKS & DOOR SHUT
34	DRIVE.PRESENT-	GND LINE ON DISK PULLS THIS LOW
35	RFSH-	
36	AB13	
37	AB11	
38	.	
39	.	
40	.	
41	.	
42	.	
43	.	
44	.	
45	.	
46	.	

```
47      .
48      .
49      .
50      .
51      .
52      .
53      .
54      .
55      .
56      .
57      .
58      .
59      +5V                          VCC SUPPLY
60      +5V
61      +5V
62      GND
63      GND
64      GND
65      .
66      RAW.READ.DATA-               UNPROCESSED DATA FROM DISK
67      TRACK.0-                     INDICATES HEAD AT OUTERMOST TRACK
68      DB4
69      SPARE.OUT-                   UNUSED PIO OUTPUT
70      DIRECTION-                   HIGH=OUT
71      DB2
72      VIDEO.DISABLE-               DISALES VIDEO DURING DISK ACCESS
73      DB7
74      DR3-.(RADIAL SELECT 3-)
75      DB1
76      DR2-.(RADIAL SELECT 2-)      USER DISK RADIAL SELECT LINE
77      ENCODED.WRITE.DATA-          FM ENCODED DATA TO DISK
78      DR1-.(RADIAL SELECT 1-)
79      INT-                         OPEN DRAIN SYSTEM INTERRUPT LINE
80      SELECT.1-.(BINARY SELECT 1-)
81      DR4-.(RADIAL SELECT 4-)
82      SELECT.0-.(BINARY SELECT 0-)
83      ROM.SELECT-.(OUT)            MCB OUTPUT TO DISABLE MDC MEMORY
84      .
85      MRQ-
86      SELECT.2-.(BINARY SELECT 2-)
87      .
88      .
89      AB9
90      .
91      AB10
92      .
93      8.PHI-                       8X SYSTEM CLOCK FOR DISK TIMING
94      AB14
```

95	SG3-	SUBGROUP 3 FOR DISK SYNCHRONIZATION
96	WRITE.PROTECT-	INDICATES WRITE PROTECT TAB IS MISSING
97	AB12	
98	AB4	
99	PHI-	SYSTEM CLOCK
100	AB3	
101	AB2	
102	AB1	
103	AB0	
104	.	
105	.	
106	.	
107	GP3-	GROUP 3 FOR DISK SYNCHRONIZATION
108	GP4-	MDC PIO GROUP DECODE
109	.	
110	.	
111	IEO.MDC.PIO	DAISY CHAIN OUTPUT FROM MDC PIO
112	.	
113	.	
114	IEI.MDC.PIO	DAISY CHAIN INPUT TO MDC PIO
115	M1-	
116	RD-	
117	.	
118	.	
119	WAIT-	
120	GND	
121	GND	
122	GND	

MDC/E PIN #	SIGNAL NAME	FUNCTION
P1A1	+5V	VCC SUPPLY
P1A1	+5V	
P1A1	+5V	
P1C4	IORQ-	
P1A12	DB5	
P2A9	DR7-.(RADIAL SELECT 7-)	
P1A13	DB3	
P2C3	STEP-	
P2C12	SELECT.3-.(BINARY SELECT :	ENABLE-)
P2A3	WRITE.GATE-	
P1C26	DB6	
P1C28	DB0	
P2C9	DR6-.(RADIAL SELECT 6-)	
P2C10	DR5-.(RADIAL SELECT 5-)	
P2A2	DISK.(C/T.0)	COMPOSITE SECTOR AND INDEX MARKS
P2C15	DR0-.(RADIAL SELECT 0-)	SYSTEM DISK RADIAL SELECT LINE
P2A4	INDEX00-	SIGNAL TO MCB CTC FOR SECTOR TIMING
P1A4	WR-	
P1A27	AB7	
P1C25	AB8	
P1A28	AB5	
P1C27	AB6	
P1A19	AB15	
P2C6	READY-	INDICATES INDEX MARKS & DOOR SHUT
P2A7	DRIVE.PRESENT-	GND LINE ON DISK PULLS THIS LOW
P1A22	RFSH-	
P1C19	AB13	
P1A20	AB11	
P1C1	+5V	VCC SUPPLY
P1C1	+5V	
P1C1	+5V	
P1A32	GND	
P1A32	GND	
P1C32	GND	
P2C24	RAW.READ.DATA-	UNPROCESSED DATA FROM DISK
P2C5	TRACK.0-	INDICATES HEAD AT OUTERMOST TRACK
P1C11	DB4	
P2C7	SPARE.OUT-	UNUSED PIO OUTPUT
P2C2	DIRECTION-	HIGH=OUT
P1C13	DB2	
P2C22	VIDEO.DISABLE-	DISALES VIDEO DURING DISK ACCESS
P1A26	DB7	
P2C13	DR3-.(RADIAL SELECT 3-)	
P1A29	DB1	
P2A13	DR2-.(RADIAL SELECT 2-)	USER DISK RADIAL SELECT LINE
P2A8	ENCODED.WRITE.DATA-	FM ENCODED DATA TO DISK

P2C14	DR1-.(RADIAL SELECT 1-)	
P1C9	INT-	OPEN DRAIN SYSTEM INTERRUPT LINE
P2A5	SELECT.1-.(BINARY SELECT 1-)	
P2A10	DR4-.(RADIAL SELECT 4-)	
P2C11	SELECT.0-.(BINARY SELECT 0-)	
P1A18	MRQ-	
P2A12	SELECT.2-.(BINARY SELECT 2-)	
P1A25	AB9	
P1C20	AB10	
P1A30	8.PHI-	8X SYSTEM CLOCK FOR DISK TIMING
P1C18	AB14	
P2C23	SG3-	SUBGROUP 3 FOR DISK SYNCHRONIZATION
P2C4	WRITE.PROTECT-	INDICATES WRITE PROTECT TAB IS MISSING
P1C16	AB12	
P1C24	AB4	
P1C10	PHI-	SYSTEM CLOCK
P1C23	AB3	
P1C17	AB2	
P1C14	AB1	
P1A17	AB0	
P2C26	GP3-	GROUP 3 FOR DISK SYNCHRONIZATION
P2A25	GP4-	MDC PIO GROUP DECODE
P2A6	IEO.MDC.PIO	DAISY CHAIN OUTPUT FROM MDC PIO
P2A5	IEI.MDC.PIO	DAISY CHAIN INPUT TO MDC PIO
P1C15	M1-	
P1A5	RD-	
P1A9	WAIT-	
P2A1	GND	
P2A1	GND	
P2C1	GND	

Zilog

10340 Bubb Road
Cupertino, California 95014
Telephone (408) 446-4666
TWX 910-338-7621

Printed in U.S.A.