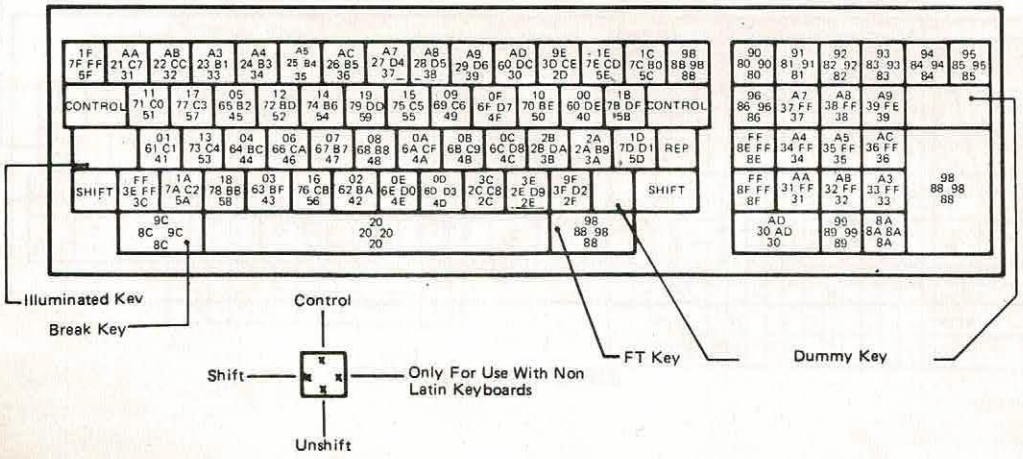
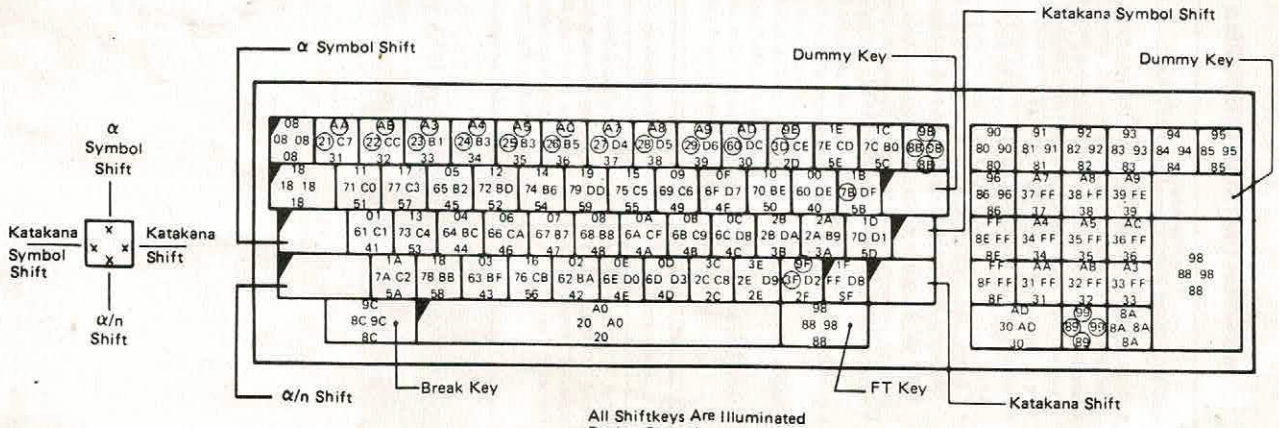
LATIN KEYBOARD CODE CHART



KATAKANA KEYBOARD CODE CHART



MONITOR INSTRUCTION FORMATS

Display/Change Memory—M,aaaa(FT Key)

- Display the next address and its contents (press the Field Terminate key)
- Change the contents of the displayed byte and display the next address and it's contents (input new byte and press the FT key)
- Terminate the function (input "," and press the FT key)
- Change the contents of the displayed byte and terminate the function (input the new byte and ","; press the FT key)

Display/Change Registers—R (FT key)

Go or Return — G (FT key)

Enable Interrupts — E (FT key)

Access Loader — L (FT key)

Response	Description
Input "1", Press FT Key	Bootload from fixed disk
Input "2", Press FT Key	Bootload from data cartridge
Input "3", Press FT Key	Bootload from flexible disk
Press FT Key	Bootload from the primary load device selected by the configuration switches

Output Memory To Data Cartridge—C (FT key)

Output Memory To Flexible Disk—F (FT key)

N, ADR FT

Access to enter a address in ROM (0-3CFF) or RAM (>3F3FF-F
FT: increments address
-FT: decrements address FBFF
,FT: leave feature return to MONITOR main routine

P (FT):

P FT

Swap flag to test RAM (00) or ROM (FF) routines

Q (FT):

Q FT

Clear RAM up from 4000 to FBFF primary 64k only

S (FT):

S FT

Start Single step feature.
Single step needs 32 Byte of CRU anywhere between A000 - F
Default value FA00 FBFF
If operator likes to change, enter

FIRMWARE ERROR CODES

Error Code	Description
	Auto-Check Diagnostics
01	A Jump instruction failed.
02	A ROM sum check instruction failed.
03	The ROM sum check failed.
04	A register instruction failed.
08	A Double Add or Load instruction failed.
09	A Load or Store instruction failed, or a read or write to the CCM RAM failed.
0A	A write instruction to the main memory between 0000 hex and 20FF (3FFF for version 3) hex failed.
0B	A read instruction from the CCM RAM failed.
0C	A read instruction from the main memory between 0000 hex and 20FF (3FFF for version 3) hex failed.
0D	A Move to Memory instruction failed.
0E	A Stack Pointer instruction failed.
0F	A Push or Pop instruction failed.
10	A Call or Return instruction failed.
11	The ROM did not transfer control for the main memory test.
1B	The first common control bus access failed.
	System Errors
13	An Internal interrupt RST 4 occurred.
14	An Internal interrupt RST 6 occurred.
15	A transfer error occurred.
16	A parity error occurred.
17	A time-out error occurred.
18	A power-down interrupt occurred.

T, ADR FT

ADR. (FT):

The trapcounter is incremented and the entered address is placed into corresponding location of trap table. Counter condition and the whole trap table is displayed. Up to 4 trap addresses may be entered, further will be ignored and the FULL message is then issued.
Starting this feature is performed with S (FT), but be aware that correct Programcounter and Stackpointer are set (use R). Now single stepping is automatically performed with displaying of all Registers and Commands before execution, until one of the entered Trap addresses will be recognized. Interruption is possible anywhere with depressing any key, but not (FT).

FT If trap addresses are already set, they can be made operative again entering only.

T FT
U, ADR FT
U FT
or

(ft) has the same efficiency as the "T"-feature, but during the test- loops no display of registers and screen rolling is performed, unless one of the valid Trap-addresses is found.
The advantage of this feature is a higher performance with approx. 100 times of speed.

O, n FT

(ft) Omit feature: n specifies the n'th trapaddress to be omitted. The trapcounter is decremented by 1 .If the omitted trapaddr.is followed by a valid address, this and also the subsequent addresses will be justified down close to the lower valid traps -if there are any- or boundary of traptable.
New contents of traptable is displayed after trapcounter,screen rolls up 1 line.
Entering O,0(ft) or 0 (ft) only,clears trapcounter and so the singlestep-loop-flag but not the trapaddresses.
With T (ft) or U (ft) they may revive.

FIRMWARE ERROR CODES (cont)

Power-Up Diagnostics	
21	A simulated read from the data cartridge failed.
22	A simulated write to the data cartridge failed.
23	The data cartridge I/F failed its power-up diagnostics.
24	The data compare failed for the data cartridge.
26	A simulated read from the fixed disk failed.
27	A simulated write to the fixed disk failed.
28	The fixed disk I/F failed its power-up diagnostics.
29	The data compare failed for the fixed disk.
2B	A simulated read from the flexible disk failed.
2C	A simulated write to the flexible disk failed.
2D	The flexible disk I/F failed its power-up diagnostics.
2E	The data compare failed for the flexible disk.
2F	No load device is selected.
32*	No errors occurred during the auto-check diagnostics.
33	No error occurred during the auto-check and power-up diagnostics.

Switch-Selectable Diagnostics	
40	No function selected.
41	No interrupt was received following a simulated keystroke
42	"No data" status was received following a simulated keystroke.
43	The Reset I/F instruction did not clear "data" status.
44	An interrupt occurred following the reset I/F instruction.
45	The Reset I/F instruction did not clear the FIFO memory.
46	The data stored in the FIFO memory is wrong.
47	The Disable Interrupts instruction failed.
48	The Reset I/F instruction did not clear the FIFO memory.
4C	No error occurred during the workstation I/F test.

* Version 3 only

PERIPHERAL ERROR CODES

ERROR XX YY ZZ

- XX = Peripheral number

Device	Peripheral Number
Interval Timer	00
Keyboard	01
Data Cartridge	02
Fixed Disk	03
Flexible Disk	05

- YY = Primary hardware status
- ZZ = Secondary hardware status

NOT READY

- Load device specified is not ready

ERROR SC 00 00

- Sum-check error

SMALL DISK POWER UP DIAGNOSTIC CODES

Primary Status	Secondary Status	Description
80	00	Failed to start the diagnostic routine
00	01	Failed data transfer between the buffer and the I/O processor board
00	02	Failed serial data transfer from the PISO register to the I/O processor board (check 1)
00	03	Failed the EXOR operation of data and the PISO register (check 1)
00	04	Failed serial data transfer from the PISO register to the I/O processor board (check 2)
00	05	Failed the EXOR operation of data and the PISO register (check 2)
00	06	Failed the PISO counter test
00	07	Failed the microprocessor test
00	08	Failed to detect a missing clock pattern
00	09	Failed to assemble the sync byte
00	0A	Failed to find the proper sync byte
00	0B	Failed to assemble the data byte
00	0C	Failed to assemble the proper data byte
00	0D	Failed to set the AA detect logic early
00	0E	Failed to force the setting of the AA detect logic
00	0F	Failed to set the timing error logic early
00	10	Failed to force the setting of the timing error logic
00	11	Failed to find the proper data in the buffer
02	00	Passed all of the power up diagnostics

FLEXIBLE DISK POWER UP DIAGNOSTIC COD

Primary Status	Secondary Status	Description
80	00	Failed to start the diagnostic routine
00	02	Master reset failed to reset the latch term
00	04	Master reset failed to set the buffer empty latch
00	07	Failed to set latch term
00	08	Master reset failed to set one of the system media latches.
00	09	Failed to set or reset the double density latch
00	0A	Failed to complete a data transfer between the two boards
00	0B	Failed to transfer an active low bit from the PC PISO register to the I/O processor board
00	0C	Failed to transfer an active high bit from the PC PISO register to the I/O processor board
00	0D	Failed to detect terminal count on the PC PISO counter
00	0E	Failed the PC generation test
00	1A	Set head load latch too soon
00	1B	Set head load latch too late
00	1F	Failed code conversion test
00	20	Failed to find a sync byte
00	21	Failed to find the proper sync byte
00	23	Failed to find the proper data byte the first time
00	24	Set the write overload latch too soon
00	25	Failed to find the proper data byte the second time
00	26	Failed to force the setting of the write overload latch
00	27	Set the read overload latch too soon
00	28	Failed to force the setting of the read overload latch

DATA CARTRIDGE POWER UP DIAGNOSTIC CODES

Secondary Status	Description
13	Write pipe error
14	CRC error
16	CRC comparison error
17	Data transfer error
18	Read pipe error
1C	Time out error
1E	Multiplexer 1 error
1F	Multiplexer 2 error

NOTE: The 3 most significant bits of the secondary status have no significance

MEMORY SAVE AREA

Memory Address In Hex	Information Stored
0070	L
0071	H
0072	E
0073	D
0074	C
0075	B
0076	Flags
0077	Accumulator
0078	Program Counter (LSB)
0079	Program Counter (MSB)
007A	Stack Pointer (LSB)
007B	Stack Pointer (MSB)
007C	Memory Address in Error (MSB)
007D	Memory Address in Error (LSB)
007E	Observed Data
007F	Expected Data

RESTART VECTORS

Restart Vector	Function
0	Reset (Power-Up or System)
1	Power-Down
2	Parity/Time-Out/Transfer Errors
3	System Interrupt (Monitor)
4	Not Used
5	Interval Timer
6	Not Used
7	External Interrupts (Peripherals)

V,nsss FF

(t) Load object feature from any disk device which is primary load device.
Device type is demanded from configuration switch on MSIF.
"n" means unit number (0...7 for fix disks resp. 0...3 for flex. disks).
"ssss" means start sector number of object file to be loaded. This number can be get via "DISPLAY" utility.
The object file should be generated by "PKE580"-assembler in packed format or NCR unpacked format with 80,480 record/block-size organization! RAP80 generated objects in unpacked format can be put on disk with the "EDIT"-utility ,but all records in front of file starting not with ":" must be deleted before storing by SA 80(80,480). 80 is the logical assignment of object file on disk.
To separate packed/unpacked formats during load feature, a flag must be set by "P" feature(see above): 00 means packed, FF means unpacked formats. Be assure that correct flag is set, before the "V,nsss"-feature is started!
Wrong entries lead to "NO OJECT" or "DISK ANDRT" message, correct performance and recognition of "Null"-record will end in "COMPLETE" message and transfer to MONITOR control is done.

CONFIGURATION SWITCH SETTINGS

Switch	Bit Position	Set (1) State	Reset (0) State
SW1 Bottom	Bit 0	12-Inch CRT	9-Inch CRT
	Bit 1	Not Used	Not Used
	Bit 2	Flexible Disk is Primary Load Device	Flexible Disk is not Primary Load Device
	Bit 3	Fixed Disk is Primary Load Device	Fixed Disk is not Primary Load Device
SW2 Top	Bit 0	Data Cartridge is Primary Load Device	Data Cartridge is not Primary Load Device
	Bit 1	Battery Back-up for the CMM Memory	No Battery Back-up for the CMM Memory
	Bit 2	Not used	Not used
	Bit 3*	Disk 1 Selected	Disk 0 Selected

*Bit 3 is only used when the Fixed Disk is the primary load device.

SERVICE REQUEST IDENTIFICATION

Bus Master	Master Identification	Poll Request	Priority
DMA	6	6	First
CCM	5	5	Last

Peripheral Or Module	CCM Poll/ Service Request Identification	DMA Poll/ Service Request Identification
Common Control Module		
Workstation Interface		
Keyboard	8	
Printer	6	
Data Cartridge	14	5
Fixed/6560 Disk	12	9
Direct Memory Access		
CRT		
Cassette		
Flexible Disk	4	7
Auxiliary Printer	10	3
Message Level Adapter	7	
	3	6

M250-07-001
In House Ad.

5 6

CCM INSTRUCTION ADDRESSES

Address	Read/ Write	Data	Instruction
FC00	R	--	Read Interrupt Status
FC03	R	--	Read Interval Timer Count
FC03	W	01-FF	Set Interval Timer Count
FC04	W	01	Enable On-Board-Memory
FC04	W	00	Disable On-Board-Memory
FC04	W	04	Enable Memory Address Translator Control
FC05	R	--	Read Nonmaskable Interrupt Status
FC05	W	00	Reset Nonmaskable Interrupt Status
FC06	R	--	Read CCM Indicator Board Lights
FC06	W	00-FF	Set CCM Indicator Board Lights

WORKSTATION INTERFACE INSTRUCTION ADDRESSES

SYSTEM CONTROL PANEL		
Address	**Data**	**Instruction**
FC21	–	Read Status
FC23	–	Read System Configuration
FC27	–	Reset Interface
PRINTER		
Address	**Data**	**Instruction**
FC30	00-7F	Write Data
FC30	–	Read Data
FC31	–	Read Status
FC32	–	Enable Interrupts
FC32	–	Read Data Turnaround
FC33	–	Disable Interrupts
FC37	–	Reset Interface
KEYBOARD		
Address	**Data**	**Instruction**
FC28	00-7F	Write Data
FC28	–	Read Data
FC29	–	Clear ENA
FC29	–	Read Status
FC2A	–	Enable Interrupts
FC2B	–	Disable Interrupts
FC2C	–	Reset Service Request
FC2D	–	Diagnostic Clear
FC2E	–	Bell
FC2F	–	Reset Interface

AUXILIARY PRINTER INTERFACE INSTRUCTION ADDRESSES

PRINTER		
Address	Data	Instruction
FDD0	00-7F	Write Data
FDD0	—	Read Data
FDD1	—	Read Status
FDD2	—	Enable Interrupts
FDD2	—	Read Data Turnaround
FDD3	—	Disable Interrupts
FDD7	—	Reset Interface

DATA CARTRIDGE INSTRUCTION ADDRESSES

FUNCTION INSTRUCTIONS		
Address	Data	Instruction
FC41	00	Rewind
FC41	01	Unload
FC41	02	Write Tapemark
FC41	03	Backspace Erase
FC41	04	Backspace IRG
FC41	05	Search Forward
FC41	06	Forward Erase
FC41	07	Write Data
FC41	08	Read Data
FC41	0A	Select Track 1
FC41	1A	Select Track 2
FC41	2A	Select Track 3
FC41	3A	Select Track 4
FC41	0E	Select Unit O
FC41	1E	Select Unit 1
FC41	09	Retension Tape
FC45	—	Read Functional Status
FC42	—	Read Diagnostic Status
FC43	—	Enable Interrupt
FC46	—	Disable Interrupt
FC47	—	Reset Service Request
		Reset Controller

DIAGNOSTIC INSTRUCTIONS		
Address	Data	Instruction
FC45	01	Run Forward
FC45	02	Run Reverse
FC45	03	Fast Forward
FC45	04	Fast Reverse
FC45	05	Stop Transport
FC45	06	Read Square Wave (Forward)
FC45	16	Read Square Wave (Reverse)
FC45	07	Start 242.2 ms Delay
FC45	09	Acceleration Adjust (Forward)
FC45	19	Acceleration Adjust (Reverse)
FC45	0B	Write Square Wave
FC45	0D	Simulated Read
FC45	0E	Simulated Write

FIXED DISK INSTRUCTION ADDRESSES

FUNCTION INSTRUCTIONS		
1ST BYTE		
Address	Data	Instruction
FC61	00	Restore
FC61	01	Seek
FC61	02	Write Format
FC61	03	Read Format
FC61	04	Write Data
FC61	05	Read Data
FC61	06	Time Disk
FC61	07	Seek RT
FC61	08	Fill Buffer
FC61	09	Dump Buffer
FC61	0A	Data Turnaround
FC61	0B	Byte Turnaround

2ND BYTE				
		Selects		
Address	Data	Drive No.	Disk No.	Software No.
FC61	00	1	0	0
FC61	01	1	1	1
FC61	02	2	0	2
FC61	03	2	1	3
FC61	04	3	0	4
FC61	05	3	1	5
FC61	06	4	0	6
FC61	07	4	1	7

3RD BYTE		
Address	Data	Comment
FC61	00-FF	Sector Address (LSB)

4TH BYTE		
Address	Data	Comment
FC61	00-3F	Sector Address (MSB)

NON- FUNCTION INSTRUCTIONS	
Address	Instruction
FC62	Enable Interrupt
FC63	Disable Interrupt
FC64	Reset Service Request
FC67	Reset
FC61	Sense 1
FC62	Sense 2

AUXILIARY PRINTER INTERFACE INSTRUCTION ADDRESSES

PRINTER		
Address	Data	Instruction
FDD0	00-7F	Write Data
FDD0	—	Read Data
FDD1	—	Read Status
FDD2	—	Enable Interrupts
FDD2	—	Read Data Turnaround
FDD3	—	Disable Interrupts
FDD7	—	Reset Interface

DATA CARTRIDGE INSTRUCTION ADDRESSES

FUNCTION INSTRUCTIONS		
Address	Data	Instruction
FC41	00	Rewind
FC41	01	Unload
FC41	02	Write Tapemark
FC41	03	Backspace Erase
FC41	04	Backspace IRG
FC41	05	Search Forward
FC41	06	Forward Erase
FC41	07	Write Data
FC41	08	Read Data
FC41	0A	Select Track 1
FC41	1A	Select Track 2
FC41	2A	Select Track 3
FC41	3A	Select Track 4
FC41	0E	Select Unit 0
FC41	1E	Select Unit 1
FC41	09	Retension Tape
FC41	—	Read Functional Status
FC45	—	Read Diagnostic Status
FC42	—	Enable Interrupt
FC43	—	Disable Interrupt
FC46	—	Reset Service Request
FC47	—	Reset Controller

DIAGNOSTIC INSTRUCTIONS		
Address	Data	Instruction
FC45	01	Run Forward
FC45	02	Run Reverse
FC45	03	Fast Forward
FC45	04	Fast Reverse
FC45	05	Stop Transport
FC45	06	Read Square Wave (Forward)
FC45	16	Read Square Wave (Reverse)
FC45	07	Start 242.2 ms Delay
FC45	09	Acceleration Adjust (Forward)
FC45	19	Acceleration Adjust (Reverse)
FC45	0B	Write Square Wave
FC45	0D	Simulated Read
FC45	0E	Simulated Write

FIXED DISK INSTRUCTION ADDRESSES

FUNCTION INSTRUCTIONS		
1ST BYTE		
Address	Data	Instruction
FC61	00	Restore
FC61	01	Seek
FC61	02	Write Format
FC61	03	Read Format
FC61	04	Write Data
FC61	05	Read Data
FC61	06	Time Disk
FC61	07	Seek RT
FC61	08	Fill Buffer
FC61	09	Dump Buffer
FC61	0A	Data Turnaround
FC61	0B	Byte Turnaround

2ND BYTE				
		Selects		
Address	Data	Drive No.	Disk No.	Software No.
FC61	00	1	0	0
FC61	01	1	1	1
FC61	02	2	0	2
FC61	03	2	1	3
FC61	04	3	0	4
FC61	05	3	1	5
FC61	06	4	0	6
FC61	07	4	1	7

3RD BYTE		
Address	Data	Comment
FC61	00-FF	Sector Address (LSB)

4TH BYTE		
Address	Data	Comment
FC61	00-3F	Sector Address (MSB)

NON-FUNCTION INSTRUCTIONS	
Address	Instruction
FC62	Enable Interrupt
FC63	Disable Interrupt
FC64	Reset Service Request
FC67	Reset
FC61	Sense 1
FC62	Sense 2

FLEXIBLE DISK INSTRUCTION ADDRESSES

FUNCTION INSTRUCTIONS

Byte	D7	D6	D5	D4	D3	D2	D1	D0	Meaning
1	C	C	0	0	F	F	F	F	Conversion/Function
2	D	O	0	0	O	U	U	H	Density/Unit/Head
3	0	T	T	T	T	T	T	T	Track Number (0-76
4	0	0	0	S	S	S	S	S	Sector Number (1-26

1ST BYTE

Address	Data	Instruction
FD01	X0	Restore
FD01	X1	Write Format
FD01	X2	Read Format
FD01	X3	Write Data
FD01	X4	Read Data
FD01	X5	Write Deleted Sector
FD01	X6	Format Defective Track
FD01	X7	Verify
FD01	X8	DMA Byte Out
FD01	X9	DMA Byte In
FD01	XA	Byte Turnaround
FD01	XB	Data Turnaround

X = 0 For No Conversion
8 For ASCII To EBCDIC
C For EBCDIC To ASCII

2ND BYTE

Address	Data	Selects	
		Unit No.	Head No.
FD01	Y0	0	0
FD01	Y1	0	1
FD01	Y2	1	0
FD01	Y3	1	1
FD01	Y4	2	0
FD01	Y5	2	1
FD01	Y6	3	0
FD01	Y7	3	1

Y = 0 For Single Density
8 For Double Density

NON-FUNCTION INSTRUCTIONS

Address	Instruction
FD01	Sense 1
FD02	Sense 2
FD02	Enable Interrupt
FD03	Disable Interrupt
FD04	Reset Service Request
FD07	Reset Controller

Peripheral	Address	Byte No.
Flexible Disk	FC8C	0
	FC8D	1
	FC8E	2
	FC8F	3
Data Cartridge	FC94	0
	FC95	1
	FC96	2
	FC97	3
Cassette	FC9C	0
	FC9D	1
	FC9E	2
	FC9F	3
Fixed/6660 Disk	FCA4	0
	FCA5	1
	FCA6	2
	FCA7	3

DMA INSTRUCTION ADDRESSES

Byte 3								Byte 2							
C1	C0	A17	A16	F11	F10	F9	F8	F7	F6	F5	F4	F3	F2	F1	F0

Byte 1								Byte 0							
A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0

C1	C0	Meaning
0	0	Transfer Error Detected
0	1	Parity Error Detected
1	0	Write Memory
1	1	Read Memory
A0 - A17		Memory Address
F0 - F11		Field Length

CRT INSTRUCTION ADDRESSES

Address	Data	Instruction
FCC0	00-1F	Write Cursor X
FCC0	—	Read Cursor X
FCC1	00-0F	Write Cursor Y
FCC1	—	Read Cursor Y
FCC2	00-7F	Write Display Character
FCC2	—	Read Display Character
FCC3	00-E0	Write Control Character
FCC3	—	Read Control Character

CASSETTE INSTRUCTION ADDRESSES

WRITE FUNCTION 1 INSTRUCTIONS

Main Drive Address	Alternate Drive Address	Data Lines	Instruction
FCE8	FCE0	01	Go Alternate Drive
FCE8	FCE0	02	Go Main Drive
FCE8	FCE0	04	Reverse Direction
FCE8	FCE0	08	Fast
FCE8	FCE0	10	Read Enable
FEC8	FCE0	20	Read Interrupt Enable
FCE8	FCE0	40	Write Interrupt Enable
FCE8	FCE0	80	Write Enable

WRITE FUNCTION 2 INSTRUCTIONS

Main Drive Address	Alternate Drive Address	Data Lines	Instruction
FCE9	FCE1	00	I/O Transfer
FCF9	FCE1	01	DMA Transfer

OTHER INSTRUCTIONS

Main Drive Address	Alternate Drive Address	Data Lines	Instruction
FCEF	FCE7	—	Read Adaptor Status
FCED	FCE4	—	Read Drive Status
FCEA	FCE2	—	Read Data
FCEB	FCE3	—	Write Data

TIME OF DAY CLOCK INSTRUCTION ADDRESSES

Address	Read/Write	Data	Instruction
FDE0	R/W	BCD	Read or set minutes
FDE1	R/W	BCD	Read or set hours
FDE2	R	*see status chart	Read power out status
FDE3	W	—	Reset power out status

INPUT TO MESSAGE LEVEL SYNCRONOUS ADAPTER (M250-05-STD)

FDA0 -- DATA OUTPUT
FDA1 -- FUNCTION 1

Function Bit Configuration								Function I Byte Description (FDA1)	
D7	D6	D5	D4	D3	D2	D1	D0	Function	
X	1	X	X	X	0	0	1	DMA Input	Received Data is transferred to the parent unit through the DMA channel
X	1	X	X	X	0	1	0	Character Input	Received Data is transferred to the parent unit through I/O port FDA0 (Diagnostics)
X	1	X	X	X	1	X	0	DMA Output	Output Data is transferred from the parent unit through the DMA channel
X	1	X	X	1	0	X	X	Character Output	Output Data is transferred from the parent unit through I/O port FDA0 (Diagnostics)
X	1	X	1	X	X	X	X	Last Buffer	The output buffer is terminated with an EOM character
X	1	X	0	X	X	X	X		The output buffer is not terminated with an EOM character
X	X	1	X	X	X	X	X	Clear	Sets the adapter into the IDLE state
X	1	X	X	X	X	X	X	Connect	Raises interchange circuit 108.2/CD
X	0	X	X	X	X	X	X		Circuit 108.2/CD is dropped. Receiver and Transmitter disabled.
1	X	X	X	X	X	X	X	New Sync	Raises interchange circuit NEW SYNC

FDA2 – FUNCTION 2

Fucntion Bit Configuration								Function 2 Byte Description (FDA2)	
D7	D6	D5	D4	D3	D2	D1	D0	Function	
X	X	X	X	X	X	X	1	Load Parameters	The adapter disables the transmitter and Receiver
X	X	X	X	X	X	X	0		The data received from the parent unit is transmitted
X	X	1	X	X	X	X	0	Loop I Turnaround	The adapter links the output data line to the input data line at the DCE interface
X	X	0	X	X	X	X	0		The adapter transmits and receives normally
X	1	X	X	X	X	X	0	Input Escape Mode	The adapter is transparent to the input data. Error checking is disabled.
X	0	X	X	X	X	X	0		Error checking is abled. The adapter operates as specified by function bits and parameters
1	X	X	X	X	X	X	0	Output Escape Mode	The adapter is transparent to the output data.
0	X	X	X	X	X	X	0		The adapter operates as specified by function bits and parameters

FDA3 -- FUNCTION 3

Function Bit Configuration								Function 3 Byte Description (FDA3)	
D7	D6	D5	D4	D3	D2	D1	D0	Function	
0	X	0	0	X	X	X	1	ASCII/EBCDIC Select	Selects ASCII code set and error protection
0	X	0	0	X	X	X	0		Selects EBCDIC code set and error protection
0	X	0	0	X	X	0	X	BSC Procedure Select	Selects BSC Procedure
0	X	0	0	X	1	X	X	Transparency Installed	Code independent (transparent) text is allowed on receive and transmitt
0	X	0	0	X	0	X	X		Code independent text is not allowed for ASCII-BSC
0	X	0	0	1	X	X	X	DLE Insert/ Remove	DLE will be inserted between the previous and current character
0	X	0	0	0	X	X	X		DLE will be removed when DLE DLE sequence is received
0	1	0	0	X	X	X	X	Control state	Forces the adapter to enter the control state

FDA4 -- ADAPTER RESET

Function -- Resets the adapter hardware and puts the adapter CPU in a stopped state.

FDA5 -- ADAPTER INITIALIZE

Function -- Forces the adapter to perform a self test routine, set the appropriate bits in statis 3, and generate a service request.

FDA6 -- MODEM CONTROL

Control Bit Configuration								Modem Control Byte Description (FDA6)	
D7	D6	D5	D4	D3	D2	D1	D0	Function	
X	X	X	X	X	X	1	X	Spare Driver	Forces the output of the spare DTE to DCE driver on
X	X	X	X	X	X	0	X		Forces the output of the spare DTE to DCE driver off
X	X	X	X	1	X	X	X	Wrap Control	Circuit 141 (local loop back) to the DCE is turned on (Loop 3 test)
X	X	X	X	0	X	X	X		Circuit 141 is turned off
1	X	X	X	X	X	X	X	Rate Selector	Selects the lower transmission rate of the DCE
0	X	X	X	X	X	X	X		Selects the higher transmission rate of the DCE

FDA7 -- STATUS RESET

Function -- Informs the adapter that status 1, 2, and 3 have been read by the parent unit.

OUTPUT FROM MESSAGE LEVEL ADAPTER

(M250-05-STD)

FDA0 -- DATA INPUT

FDA1 -- STATUS 1

Status Bit Configuration								Status I Byte Description (FDA1)	
D7	D6	D5	D4	D3	D2	D1	D0	Status	
X	X	X	X	X	X	X	1	Input Complete	Raised when the adapter receives an EOM character
X	X	X	X	X	X	1	X	Input Terminate	Raised on DMA input when DMA controller sends Terminate on character input for each character
X	X	X	X	X	1	X	X	Output Complete	Raised when the adapter receives the last character from the parent unit
X	X	X	X	1	X	X	X	Output Terminate	Raised on DMA output and character output on terminate signal
X	X	X	1	X	X	X	X	Transparent Text	The input buffer contains transparent text
X	X	X	0	X	X	X	X	Received	The input buffer does not contain transparent text
X	1	X	X	X	X	X	X	Status 2 Flag	Indicates that 1 or more bits are set in status 2
1	X	X	X	X	X	X	X	Status 3 Flag	Indicates that 1 or more bits are set in status 3

FDA2 -- STATUS 2

Status Bit Configuration								Status 2 Byte Description (FDA2)	
D7	D6	D5	D4	D3	D2	D1	D0	Status	
X	X	X	X	X	X	X	1	Input Error	Signals errors detected during input
X	X	X	X	X	X	1	X	DLE EOT	Raised if a DLE EOT sequence is received by the adapter
X	X	X	X	X	1	X	X	Over/Under Load	Overload occurs when the adapter is not provided with another input buffer within 1 character time after the 100 byte buffer is filled. Under load occurs when the adapter times out before transmitting terminate
X	X	X	X	1	X	X	X	Input Channel Error	Raised if RLSD drops during input or while carrier Flag 2 is set
X	X	X	1	X	X	X	X	Output Channel Error	Raised if RFS does not come within one transmission interval after RQS or if RFS drops during transmission
X	X	1	X	X	X	X	X	Circuit Error	Raised if DSR drops while DTR is up
X	1	X	X	X	X	X	X	EOT Received	Set when an EOT signal is received while the adapter is in input or output mode
1	X	X	X	X	X	X	X	Time Out	Set when one of the timers times out

FDA3 -- STATUS 3

Status Bit Configuration								Status 3 Byte Description (FDA3)	
D7	D6	D5	D4	D3	D2	D1	D0	Status	
X	X	X	X	X	X	X	1	Connected	Set on an OFF to ON transition of DSR after CONNECT has been set
X	X	X	X	X	X	1	X	Wrap Indicator Flag	Set on a transition of the wrap indicator
X	X	X	X	X	1	X	X	Poll Sequence Received	Set when the adapter has received and validated a poll sequence
X	X	X	X	1	X	X	X	Select Sequence Received	Set when the adapter has received and validated a select sequence
X	X	X	1	X	X	X	X	Test Completed	Set when the adapter terminates Level 0 diagnostics after initialization

Test Result Code								Meaning Of Code
0	0	1	1	X	X	X	X	ROM (CRC) error
0	1	0	1	X	X	X	X	RAM Read/Write error
0	1	1	0	X	X	X	X	Interval Timer error
1	0	0	1	X	X	X	X	USART/Timer error
1	0	1	1	X	X	X	X	USART Loop 1 Turnaround error
1	1	0	1	X	X	X	X	(Optional) Loop 3 Turnaround error
1	1	1	1	X	X	X	X	All tests successfully completed

FDA4 -- STRAPPING BYTE 1
FDA5 -- STRAPPING BYTE 2

NOTE: Strapping bytes 1 and 2 are intended for use as Poll and Select identification strapping

FDA6 -- MODEM STATUS

Status Bit Configuration								Modem Status Byte Description (FDA6)	
D7	D6	D5	D4	D3	D2	D1	D0	Status	
X	X	X	X	X	X	X	1	Received Line Signal Detector	Indicates an ON condition of circuit 109/CF
X	X	X	X	X	X	X	0		Indicates an OFF condition of circuit 109/CF
X	X	X	X	X	X	1	X	Data Set Ready	Indicates an ON condition of circuit 107/CC
X	X	X	X	X	X	0	X		Indicates an OFF condition of circuit 107/CC
X	X	X	X	X	1	X	X	Calling Indicator	Indicates an ON condition of circuit 125/CE
X	X	X	X	X	0	X	X		Indicates an OFF condition of circuit 125/CE
X	X	X	X	1	X	X	X	Wrap Indicator	Indicates an ON condition of circuit 142 (Test indicator)
X	X	X	X	0	X	X	X		Indicates an OFF condition of circuit 142 (Test indicator)
X	X	X	1	X	X	X	X	Ready For Sending	Indicates an ON condition of circuit 106/CB
X	X	X	0	X	X	X	X		Indicates an OFF condition of circuit 106/CB
X	X	1	X	X	X	X	X	Request To Send	Indicates an ON condition of circuit 105/CA
X	X	0	X	X	X	X	X		Indicates an OFF condition of circuit 105/CA
X	1	X	X	X	X	X	X	Data Terminal Ready	Indicates an ON condition of circuit 108.2/CD
X	0	X	X	X	X	X	X		Indicates an OFF condition of circuit 108.2/CD
1	X	X	X	X	X	X	X	Loop 1 Activated	The adapter is set up for a Loop 1 turnaround test
0	X	X	X	X	X	X	*X		The adapter transmits and receives normally

LINE PRINTER HARDWARE STATUS

Primary Status Bit Configuration								Status Byte Description
D7	D6	D5	D4	D3	D2	D1	DO	
1	X	X	X	X	X	X	X	The printer is busy.
X	1	X	X	X	X	X	X	The printer is not ready.
X	X	X	X	X	1	X	X	The printer is out of paper.
X	X	X	X	1	X	X	X	A data transmission error occurred between the workstation I/F and printer.
X	X	X	X	X	X	1	X	A data transmission between the workstation I/F and the printer has started, but it is not finished.
NOTE: Bit positions with an X have no significance.								

CCM HARDWARE STATUS

Maskable Interrupt Status								
D7	D6	D5	D4	D3	D2	D1	D0	Status Description
X	X	1	0	0	1	1	1	Internal Interrupt Level 4
X	X	1	0	1	1	1	1	Internal Interrupt Level 5
X	X	1	1	0	1	1	1	Internal Interrupt Level 6
X	1	X	X	X	1	1	1	Maskable Interrupts Are Disabled
X	0	X	X	X	1	1	1	Maskable Interrupts Are Enabled
1	X	X	X	X	1	1	1	Internal Interrupt Waiting
0	X	X	X	X	1	1	1	Internal Interrupt Not Waiting
Nonmaskable Interrupt Status								
X	X	X	X	1	X	X	X	On-Board-Memory Enabled
X	X	X	X	X	1	X	X	Time-Out Error Interrupt
X	X	X	X	X	X	1	X	Parity Error Interrupt
X	X	X	X	X	X	X	1	Transfer Error Interrupt

NOTE: Bit Positions with an X have no signifigance

TIME OF DAY CLOCK POWER OUT STATUS

D7	D6	D5	D4	D3	D2	D1	D0	* Power Out Status
X	X	X	X	X	0	0	0	Power out less than 1 day
X	X	X	X	X	0	0	1	Power out 1 day
X	X	X	X	X	0	1	0	Power out 2 days
X	X	X	X	X	0	1	1	Power out 3 days
X	X	X	X	X	1	0	0	Power out excessive

DATA CARTRIDGE HARDWARE STATUS

Primary Status Bit Configuration								Status Byte Description
D7	D6	D5	D4	D3	D2	D1	DO	
X	X	X	X	X	X	X	1	The CCM poll request is enabled.
X	X	X	X	X	X	1	X	The controller is not busy.
X	X	X	X	X	1	X	X	Early warning or load point hole was detected.
X	X	X	X	1	X	X	X	Data cartridge drive not ready.
X	X	X	1	X	X	X	X	An error occurred during a function instruction.
X	X	1	X	X	X	X	X	A read instruction did not find data before 1.5 seconds.
X	1	X	X	X	X	X	X	Data can be written on the tape (not safe).
1	X	X	X	X	X	X	X	A tapemark was read from the tape.

Secondary Status Bit Configurations								Status Byte Description
X	X	X	0	0	1	1	0	The CRC bytes did not compare in the read after write check.
X	X	X	0	0	1	0	0	A CRC error occurred in a read data instruction.
X	X	X	0	0	1	1	1	A DMA transfer did not occur in the required time.
X	X	X	0	1	0	0	0	The load point hole was detected during a backspace IRG or erase instruction.
X	X	X	0	0	0	1	1	An error occurred while writing or reading a tapemark.
X	X	X	0	1	1	0	0	A time-out error occurred.
X	X	X	0	1	0	1	1	The end of the tape was detected.
X	X	X	0	1	1	1	0	The data cartridge is not in the drive.
X	X	1	0	X	X	X	X	The upper tape hole sensor is not active.
X	1	X	0	X	X	X	X	The lower tape hole sensor is not active.
1	X	X	0	X	X	X	X	The tape is at the load point position.
NOTE: Bit positions with an X have no significance.								

FIXED DISK HARDWARE STATUS

Primary Status Bit Configuration								Status Byte Description
D7	D6	D5	D4	D3	D2	D1	DO	
1	X	X	X	X	X	X	X	The controller is active.
X	1	X	X	X	X	X	X	The CCM poll request line is active.
0	0	X	1	0	0	0	0	A write data or write format instruction was received for a write-protected disk platter.
0	0	X	0	1	0	0	0	The disk drive selected is not ready.
0	0	X	0	0	1	0	0	The CCM sent an invalid instruction to the controller.
0	0	X	0	0	0	1	0	The operation completed successfully.
0	0	X	0	0	0	0	1	A soft error occurred.
0	0	0	0	0	0	0	0	The controller failed the power-up diagnostics, or it can not determine the cause of the error.

Secondary Status Bit Configuration								Status Byte Description
1	X	X	X	X	X	X	X	An alternate track was used during the last operation.
X	1	X	X	X	X	X	X	A parity error occurred during a DMA transfer.
X	X	1	X	X	X	X	X	A polynomial check error occurred in an address or data field.
X	X	X	1	X	X	X	X	A missing clock was detected in a data field.
X	X	X	X	1	X	X	X	A data sync byte was not found during a read operation.
X	X	X	X	X	1	X	X	The calculated sector was not found.
X	X	X	X	X	X	1	X	A fault error occurred in the selected disk drive.
X	X	X	X	X	X	X	1	A seek error occurred in the selected disk drive.

NOTE: Bit positions with an X have no significance.

FLEXIBLE DISK HARDWARE STATUS

Primary Status Bit Configuration								Status Byte Description
D7	D6	D5	D4	D3	D2	D1	DO	
1	O	X	X	X	X	X	X	The controller is active.
1	1	X	X	X	X	X	X	The CCM poll request line is active.
O	O	1	X	X	X	X	X	A deleted sector mark was found during a read data or verify instruction.
O	O	X	X	O	O	O	O	The controller failed the power-up diagnostics, or it can not determine the cause of the error.
O	O	X	X	O	O	O	1	A soft error occurred.
O	O	X	X	O	O	1	O	The operation completed successfully.
O	O	X	X	O	O	1	1	The CCM sent an invalid instruction to the controller.
O	O	X	X	O	1	O	O	The disk drive selected is not ready.

O	O	X	X	O	1	O	1	The media in the specified drive was removed and inserted again since the last instruction to this drive.
O	O	X	X	O	1	1	1	A verify error occurred.
O	O	X	X	1	O	O	O	A read or write instruction was tried above sector 26 of track 73.
Secondary Status Bit Configuration								**Status Byte Description**
X	1	X	X	X	X	X	X	A parity error occurred during a DMA transfer.
X	X	1	X	X	X	X	X	A polynomial check error occurred in an address or data field.
X	X	X	1	X	X	X	X	A DMA transfer did not occur in the required time.
X	X	X	X	1	X	X	X	The controller failed to find the data mark during a read data or verify instruction.
X	X	X	X	X	1	X	X	The specified sector was not found between 2 index pulses.
X	X	X	X	X	X	1	X	A seek error occurred.
X	X	X	X	X	X	X	1	A write fault was detected from the selected drive.
NOTE: Bit positions with an X have no significance.								

CASSETTE HARDWARE STATUS

Adapter Status Bit Configuration								Status Byte Description
D7	D6	D5	D4	D3	D2	D1	DO	
1	X	X	X	X	X	X	X	The B-EOT or clear leader interrupt is active.
X	1	X	X	X	X	X	X	The data interrupt is active.
X	X	1	X	X	X	X	X	A CRC error occurred.
X	X	X	1	X	X	X	X	An EOB was reached.
X	X	X	X	1	X	X	X	A DMA parity error occurred.
X	X	X	X	X	1	X	X	The DTC and DMA select lines are active.
X	X	X	X	X	X	1	X	A read or write interrupt was not acknowledged within 1.33 msec.

Transport Status Bit Configuration								Status Byte Description
X	X	X	1	X	X	X	X	The BOT/EOT hole or clear leader/trailer is present over the photoelectric sensor.
X	X	X	X	1	X	X	X	The B side of the cassette is up.
X	X	X	X	X	1	X	X	Data can be written on the tape.
X	X	X	X	X	X	1	X	The selected transport is ready.
X	X	X	X	X	X	X	1	The lid of the selected transport is open.
NOTE: Bit positions with an X have no significance.								

VISUAL RECORD PRINTER HARDWARE STATUS

Primary Status Bit Configuration								Status Byte Description
D7	D6	D5	D4	D3	D2	D1	D0	
X	1	X	X	X	X	X	X	The printer is not ready.
X	X	X	X	X	X	X	1	The status of the printer changed, or the next bar code bit is ready to be transferred.
X	X	X	X	1	X	X	X	A data transmission error occurred between the workstation I/F and the printer.
X	X	X	X	X	X	1	X	A data transmission between the workstation I/F and the printer started, but it is not finished.

NOTE: Bit positions with an X have no significance.

KEYBOARD HARDWARE STATUS

Bit Meaning	Status Bits							
	D7	D6	D5	D4	D3	D2	D1	D0
Entry Not Accepted	X	0	1	0	X	X	X	X
Data	X	0	0	1	X	X	X	X
Break	X	1	0	0	X	X	X	X

NOTE: Bit positions with an X have no significance.

ERROR LOG RECORD TYPES

- 01—Fixed or NCR 6560 disk error
- 10—Flexible disk error
- 20—An error was detected by the on-line communication driver.
- 25—Tally information for the ratio between the number of messages received with errors and the total number of messages received.
- 26—Tally information for the ratio between the number of messages retransmitted and the total number of messages transmitted.
- 27—An error during a loop 1 test.
- 28—An error during a loop 3 test.
- 29—The capacity of the data capture buffer has been exceeded (wrap-around condition).
- 40—Cassette error
- 5X—Visual record printer error
- 60—Data transmission error detected from the matrix line printer
- 61—Time-out error detected from the matrix line printer
- 81—Data cartridge module error
- 82—Data cartridge tape is at the load point when it should not be
- 83—Time-out error detected from the data cartridge
- 84—Power failure detected from the data cartridge
- 85—Data error detected from the data cartridge
- 90—System patcher information

ERROR LOG FUNCTION CODES

Function Code In Hex	Device					
	Data Cartridge	Cassette	Fixed/6560 Disk	Flexible Disk	Line Printer	Visual Record Printer
0						
1	Read Data	Read Data	Read Data	Read Data		
2	Write Data	Write Data	Write Data	Write Data		Read Barcode
3					Print After Line Advance	Print or Read After Write
4						
5						
6	Backspace Erase	Backspace Erase		Write Deleted Sector		

7	Search Forward	Search To Specific Block	Seek		Line Advance	Media Slew
8	Rewind	Rewind	Restore	Restore		
9	Retention Tape		Read Format	Read Format		
A	Write Tapemark	Write Tapemark	Write Format	Write Format	Print Before Line Advance	
B	Unload	Unload		Verify		
C	Backspace IRG	Backspace IRG	Read Data Multiple Sectors	Read Data Multiple Sectors		
D	Read Status	Read Status				
E	Forward Erase			Write Defective Track		
F	Track Select					

FIXED DISK SECTOR CONVERSION CHART

Cyl.	Head 00	Head 01	Cyl.	Head 00	Head 01	Cyl.	Head 00	Head 01
0	0000	0012	60	1440	1452	120	2880	2892
1	0024	0036	61	1464	1476	121	2904	2916
2	0048	0060	62	1488	1500	122	2928	2940
3	0072	0084	63	1512	1524	123	2952	2964
4	0096	0108	64	1536	1548	124	2976	2988
5	0120	0132	65	1560	1572	125	3000	3012
6	0144	0156	66	1584	1596	126	3024	3036
7	0168	0180	67	1608	1620	127	3048	3060
8	0192	0204	68	1632	1644	128	3072	3084
9	0216	0228	69	1656	1668	129	3096	3108
10	0240	0252	70	1680	1692	130	3120	3132
11	0264	0276	71	1704	1716	131	3144	3156
12	0288	0300	72	1728	1740	132	3168	3180
13	0312	0324	73	1752	1764	133	3192	3204
14	0336	0348	74	1776	1788	134	3216	3228
15	0360	0372	75	1800	1812	135	3240	3252
16	0384	0396	76	1824	1836	136	3264	3276
17	0408	0420	77	1848	1860	137	3288	3300
18	0432	0444	78	1872	1884	138	3312	3324
19	0456	0468	79	1896	1908	139	3336	3348
20	0480	0492	80	1920	1932	140	3360	3372
21	0504	0516	81	1944	1956	141	3384	3396
22	0528	0540	82	1968	1980	142	3408	3420
23	0552	0564	83	1992	2004	143	3432	3444
24	0576	0588	84	2016	2028	144	3456	3468
25	0600	0612	85	2040	2052	145	3480	3492
26	0624	0636	86	2064	2076	146	3504	3516
27	0648	0660	87	2088	2100	147	3528	3540
28	0672	0684	88	2112	2124	148	3552	3564
29	0696	0708	89	2136	2148	149	3576	3588
30	0720	0732	90	2160	2172	150	3600	3612
31	0744	0756	91	2184	2196	151	3624	3636
32	0768	0780	92	2208	2220	152	3648	3660
33	0792	0804	93	2232	2244	153	3672	3684
34	0816	0828	94	2256	2268	154	3696	3708
35	0840	0852	95	2280	2292	155	3720	3732
36	0864	0876	96	2304	2316	156	3744	3756
37	0888	0900	97	2328	2340	157	3768	3780
38	0912	0924	98	2352	2364	158	3792	3804
39	0936	0948	99	2376	2388	159	3816	3828
40	0960	0972	100	2400	2412	160	3840	3852
41	0984	0996	101	2424	2436	161	3864	3876
42	1008	1020	102	2448	2460	162	3888	3900
43	1032	1044	103	2472	2484	163	3912	3924
44	1056	1068	104	2496	2508	164	3936	3948
45	1080	1092	105	2520	2532	165	3960	3972
46	1104	1116	106	2544	2556	166	3984	3996
47	1128	1140	107	2568	2580	167	4008	4020
48	1152	1164	108	2592	2604	168	4032	4044
49	1176	1188	109	2616	2628	169	4056	4068
50	1200	1212	110	2640	2652	170	4080	4092
51	1224	1236	111	2664	2676	171	4104	4116
52	1248	1260	112	2688	2700	172	4128	4140
53	1272	1284	113	2712	2724	173	4152	4164
54	1296	1308	114	2736	2748	174	4176	4188
55	1320	1332	115	2760	2772	175	4200	4212
56	1344	1356	116	2784	2796	176	4224	4236
57	1368	1380	117	2808	2820	177	4248	4260
58	1392	1404	118	2832	2844	178	4272	4284
59	1416	1428	119	2856	2868	179	4296	4308

Cyl.	Head 00	Head 01	Cyl.	Head 00	Head 01	Cyl.	Head 00	Head 01
180	4320	4332	245	5880	5892	310	7440	7452
181	4344	4356	246	5904	5916	311	7464	7476
182	4368	4380	247	5928	5940	312	7488	7500
183	4392	4404	248	5952	5964	313	7512	7524
184	4416	4428	249	5976	5988	314	7536	7548
185	4440	4452	250	6000	6012	315	7560	7572
186	4464	4476	251	6024	6036	316	7584	7596
187	4488	4500	252	6048	6060	317	7608	7620
188	4512	4524	253	6072	6084	318	7632	7644
189	4536	4548	254	6096	6108	319	7656	7668
190	4560	4572	255	6120	6132	320	7680	7692
191	4584	4596	256	6144	6156	321	7704	7716
192	4608	4620	257	6168	6180	322	7728	7740
193	4632	4644	258	6192	6204	323	7752	7764
194	4656	4668	259	6216	6228	324	7776	7788
195	4680	4692	260	6240	6252	325	7800	7812
196	4704	4716	261	6264	6276	326	7824	7836
197	4728	4740	262	6288	6300	327	7848	7860
198	4752	4764	263	6312	6324	328	7872	7884
199	4776	4788	264	6336	6348	329	7896	7908
200	4800	4812	265	6360	6372	330	7920	7932
201	4824	4836	266	6384	6396	331	7944	7956
202	4848	4860	267	6408	6420	332	7968	7980
203	4872	4884	268	6432	6444	333	7992	8004
204	4896	4908	269	6456	6468	334	8016	8028
205	4920	4932	270	6480	6492	335	8040	8052
206	4944	4956	271	6504	6516	336	8064	8076
207	4968	4980	272	6528	6540	337	8088	8100
208	4992	5004	273	6552	6564	338	8112	8124
209	5016	5028	274	6576	6588	339	8136	8148
210	5040	5052	275	6600	6612	340	8160	8172
211	5064	5076	276	6624	6636	341	8184	8196
212	5088	5100	277	6648	6660	342	8208	8220
213	5112	5124	278	6672	6684	343	8232	8244
214	5136	5148	279	6696	6708	344	8256	8268
215	5160	5172	280	6720	6732	345	8280	8292
216	5184	5196	281	6744	6756	346	8304	8316
217	5208	5220	282	6768	6780	347	8328	8340
218	5232	5244	283	6792	6804	348	8352	8364
219	5256	5268	284	6816	6828	349	8376	8388
220	5280	5292	285	6840	6852	350	8400	8412
221	5304	5316	286	6864	6876	351	8424	8436
222	5328	5340	287	6888	6900	352	8448	8460
223	5352	5364	288	6912	6924	353	8472	8484
224	5376	5388	289	6936	6948	354	8496	8508
225	5400	5412	290	6960	6972	355	8520	8532
226	5424	5436	291	6984	6996	356	8544	8556
227	5448	5460	292	7008	7020	357	8568	8580
228	5472	5484	293	7032	7044	358	8592	8604
229	5496	5508	294	7056	7068	359	8616	8628
230	5520	5532	295	7080	7092	360	8640	8652
231	5544	5556	296	7104	7116	361	8664	8676
232	5568	5580	297	7128	7140	362	8688	8700
233	5592	5604	298	7152	7164	363	8712	8724
234	5616	5628	299	7176	7188	364	8736	8748
235	5640	5652	300	7200	7212	365	8760	8772
236	5664	5676	301	7224	7236	366	8784	8796
237	5688	5700	302	7248	7260	367	8808	8820
238	5712	5724	303	7272	7284	368	8832	8844
239	5736	5748	304	7296	7308	369	8856	8868
240	5760	5772	305	7320	7332	370	8880	8892
241	5784	5796	306	7344	7356	371	8904	8916
242	5808	5820	307	7368	7380	372	8928	8940
243	5832	5844	308	7392	7404	373	8952	8964
244	5856	5868	309	7416	7428	374	8976	8988

FIXED DISK SECTOR CONVERSION CHART (cont)

Cyl.	Head 00	Head 01	Cyl.	Head 00	Head 01	Cyl.	Head 00	Head 01
375	9000	9012	386	9264	9276	397	9528	9540
376	9024	9036	387	9288	9300	398	9552	9564
377	9048	9060	388	9312	9324	399	9576	9588
378	9072	9084	389	9336	9348	400	9600	9612
379	9096	9108	390	9360	9372	401	9624	9636
380	9120	9132	391	9384	9396	402	9648	9660
381	9144	9156	392	9408	9420	403	9672	9684
382	9168	9180	393	9432	9444	404	9696	9708
383	9192	9204	394	9456	9468	405	9720	9732
384	9216	9228	395	9480	9492	406	9744	9756
385	9240	9252	396	9504	9516	407	9768	9780

FLEXIBLE DISK SECTOR CONVERSION CHART

Track Number	Starting Sector	Track Number	Starting Sector	Track Number	Starting Sector
Head No. 0		50	1301	26	2601
		51	1327	27	2627
00	0001	52	1353	28	2653
01	0027	53	1379	29	2679
02	0053	54	1405	30	2705
03	0076	55	1431	31	2731
04	0105	56	1457	32	2757
05	0131	57	1483	33	2783
06	0157	58	1509	34	2809
07	0183	59	1535	35	2835
08	0209	60	1561	36	2861
09	0235	61	1587	37	2887
10	0261	62	1613	38	2913
11	0287	63	1639	39	2939
12	0313	64	1665	40	2965
13	0339	65	1691	41	2991
14	0365	66	1717	42	3017
15	0391	67	1743	43	3043
16	0417	68	1769	44	3069
17	0443	69	1795	45	3095
18	0469	70	1821	46	3121
19	0495	71	1847	47	3147
20	0521	72	1873	48	3173
21	0547	73	1899	49	3199
22	0573	Head No.1		50	3225
23	0599			51	3251
24	0625	00	1925	52	3277
25	0651	01	1951	53	3303
26	0677	02	1977	54	3329
27	0703	03	2003	55	3355
28	0729	04	2029	56	3381
29	0755	05	2055	57	3407
30	0781	06	2081	58	3433
31	0807	07	2107	59	3459
32	0833	08	2133	60	3485
33	0859	09	2159	61	3511
34	0885	10	2185	62	3537
35	0911	11	2211	63	3563
36	0937	12	2237	64	3589
37	0963	13	2263	65	3615
38	0989	14	2289	66	3641
39	1015	15	2315	67	3667
40	1041	16	2341	68	3693
41	1067	17	2367	69	3719
42	1093	18	2393	70	3745
43	1119	19	2419	71	3771
44	1145	20	2449	72	3797
45	1171	21	2471	73	3823
46	1197	22	2497		
47	1223	23	2523		
48	1249	24	2549		
49	1275	25	2575		

NOTES

Zahlensysteme
Blatt 4: Zahlenzuordnung sedezimal ⟷ dezimal

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
1	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
2	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47
3	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63
4	64	65	66	67	68	69	70	71	72	73	74	75	76	77	78	79
5	80	81	82	83	84	85	86	87	88							

HEXADECIMAL AND DECIMAL CONVERSION

To find the decimal number, locate the Hex number and its decimal equivalent for each position. Add these to obtain the decimal number. To find the Hex number, locate the next lower decimal number and its Hex equivalent. Each difference is used to obtain the next Hex number until the entire number is developed.

Byte 4567 Hex	Byte 4567 Dec	Byte 0123 Hex	Byte 0123 Dec	Byte 4567 Hex	Byte 4567 Dec	Byte 0123 Hex	Byte 0123 Dec	Byte 4567 Hex	Byte 4567 Dec	Byte 0123 Hex	Byte 0123 Dec
0	0	0	0	0	0	0	0	0	0	0	0
1	1,048,576	1	65,536	1	4,096	1	256	1	16	1	1
2	2,097,152	2	131,072	2	8,192	2	512	2	32	2	2
3	3,145,728	3	196,608	3	12,288	3	768	3	48	3	3
4	4,194,304	4	262,144	4	16,384	4	1,024	4	64	4	4
5	5,242,880	5	327,680	5	20,480	5	1,280	5	80	5	5
6	6,291,456	6	393,216	6	24,576	6	1,536	6	96	6	6
7	7,340,032	7	458,752	7	28,672	7	1,792	7	112	7	7
8	8,388,608	8	524,288	8	32,768	8	2,048	8	128	8	8
9	9,437,184	9	589,824	9	36,864	9	2,304	9	144	9	9
A	10,485,760	A	655,360	A	40,960	A	2,560	A	160	A	10
B	11,534,336	B	720,896	B	45,056	B	2,816	B	176	B	11
C	12,582,912	C	786,432	C	49,152	C	3,072	C	192	C	12
D	13,631,488	D	851,968	D	53,248	D	3,328	D	208	D	13
E	14,680,064	E	917,504	E	57,344	E	3,584	E	224	E	14
F	15,728,640	F	983,040	F	61,440	F	3,840	F	240	F	15
	6		5		4		3		2		1

Example: Decimal 10,484 to Hex

10,484 = 10484 - 8192 = 2292 - 2048 = 244 - 240 = 4 - 4 = 0
2 8 F 4 = Hex 28F4

Example: Hex 28F4 to Decimal

28F4 = 2 + 8 + F + 4
8192 + 2048 + 240 + 4 = Decimal 10484

Powers of 16 16^n	n	Powers of 2 2^n	n
1	0	512	9
16	1	1 024	10
256	2	2 048	11
4 096	3	4 096	12
65 536	4	8 192	13
1 048 576	5	16 384	14
16 777 216	6	32 768	15
268 435 456	7	65 536	16
4 294 967 296	8	131 072	17
68 719 476 736	9	262 144	18
1 099 511 627 776	10	524 288	19
17 592 186 044 416	11	1 048 576	20
281 474 976 710 656	12	2 097 152	21
4 503 599 627 370 496	13	4 194 304	22
72 057 594 037 927 936	14	8 388 608	23
1 152 921 504 606 846 976	15	16 777 216	24

EBCDIC CODE CHART

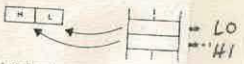
EBCDIC CODE CHART

B8-B5 \ B4-B1	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0000	NUL	SOH	STX	ETX	PF	HT	LC	DEL	GE	RLF	SMM	VT	FF	CR	SO	SI
0001	DLE	DC1	DC2	TM	RES	NL	BS	IL	CAN	EM	CC	CU1	IFS	IGS	IRS	IUS
0010	DS	SOS	FS		BYP	LF	ETB	ESC			SM	CU2		ENQ	ACK	BEL
0011			SYN		PN	RS	UC	EOT				CU3	DC4	NAK		SUB
0100	SP										¢	.	<	(	+	|
0101	&										!	$	*	)	;	¬
0110	–	/									¦	,	%	–	>	?
0111										/	:	#	@	'	=	"

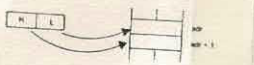
8080 / 8085

Datenbefehle

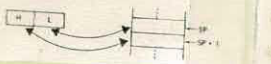
		Flags C P Z S	Zyklen
MOV r1, r2	Lade Register r1 mit Inhalt von Register r2	• • • •	1
MOV r, M	Lade Register r1 mit Inhalt des Speicherplatzes [M]	• • • •	2
MOV M, r	Lade Speicherplatz [M] mit Inhalt vom Register r1	• • • •	2
MVI r, byte	Lade Register r1 mit 8-bit Konstanten byte	• • • •	2
MVI M, byte	Lade Speicherplatz [M] mit Konstanten byte	• • • •	3
LXI rp, dbyte	Lade Registerpaar rp1 mit 16-bit Konstanten dbyte	• • • •	3
LXI SP, dbyte	Lade Stackpointer mit 16-bit Konstanten dbyte	• • • •	3
LDA adr	Lade Accumulator mit Inhalt des Speicherplatzes adr	• • • •	4
STA adr	Lade Speicherplatz adr mit Inhalt des Accumulators	• • • •	4
LHLD adr	Lade Registerpaar (H,L) mit Inhalt der Speicherplätze adr, adr + 1	• • • •	5



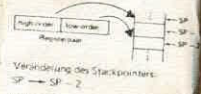
SHLD adr	Lade Speicherplätze adr, adr + 1 mit Inhalt des Registerpaares (H,L)	• • • •	5



LDAX rp2	Lade Accumulator mit Inhalt des Speicherplatzes, dessen Adresse im Registerpaar rp2 steht	• • • •	2
STAX rp2	Lade Speicherplatz, dessen Adresse im Registerpaar rp2 steht, mit Inhalt vom Accumulator	• • • •	2
SPHL	Lade Stackpointer mit Inhalt des Registerpaares (H,L)	• • • •	1
PCHL	Lade Programmcounter mit Inhalt des Registerpaares (H,L)	• • • •	1
XCHG	Vertausche Inhalte der Registerpaare (H,L) und (D,E)	• • • •	1
XTHL	Vertausche Inhalte der Stackspeicherplätze SP, SP + 1 und des Registerpaares (H,L)	• • • •	5



		Flags C P Z S	Zyklen
PUSH rp1	Schreibe Inhalt des Registerpaares rp1 in den Stack	• • • •	3



Veränderung des Stackpointers:
SP ⟶ SP − 2

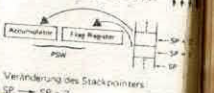
POP rp1	Hole 2-byte Inhalt aus dem Stack in das Registerpaar rp1	• • • •	3

Veränderung des Stackpointers:
SP ⟶ SP + 2

PUSH PSW	Schreibe Programm Status Wort in den Stack	• • • •	3

Veränderung des Stackpointers:
SP ⟶ SP − 2

POP PSW	Hole 2-byte Inhalt aus dem Stack	• • • •	3



Veränderung des Stackpointers:
SP ⟶ SP + 2

Arithmetische Befehle

		Flags C P Z S	Zyklen
ADD r1	Accumulator = Accumulator + Register r1	• • • •	1
ADC r2	Accumulator = Accumulator + Register r1 + Carry	• • • •	1
ADD M	Accumulator = Accumulator + [M]	• • • •	2
ADC M	Accumulator = Accumulator + [M] + Carry	• • • •	2
ADI byte	Accumulator = Accumulator + byte	• • • •	2
ACI byte	Accumulator = Accumulator + byte + Carry	• • • •	2
SUB r1	Accumulator = Accumulator − Register r1	• • • •	1
SBB r1	Accumulator = Accumulator − Register r1 − Carry	• • • •	1

Arithm.

		Flags C P Z S	Zyklen
SUB M	Accumulator = Accumulator − [M]	• • • •	2
SBB M	Accumulator = Accumulator − [M] − Carry	• • • •	2
SUI byte	Accumulator = Accumulator − byte	• • • •	2
SBI byte	Accumulator = Accumulator − byte − Carry	• • • •	2
DAD rp1	(H,L) = (H,L) + rp1 (Addition von Registerpaaren)	• • • •	3
DAD SP	(H,L) = (H,L) + SP	• • • •	3
DAA	'Decimal-Adjust' des Accumulators (nur nach BCD-Operationen)	• • • •	1
INR r1	Inkrementiere (erhöhe um 1) Register r1	• • • •	1
INR M	[M]	• • • •	3
INX rp1	Registerpaar rp1	• • • •	1
INX SP	Stackpointer	• • • •	1
DCR r1	Dekrementiere (vermindere um 1) Register r1	• • • •	1
DCR M	[M]	• • • •	3
DCX rp1	Registerpaar rp1	• • • •	1
DCX SP	Stackpointer	• • • •	1

Logische Befehle

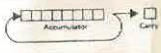
		Flags C P Z S	Zyklen
ANA r1	Accumulator = Accumulator 'AND' Register r1	0 • • •	1
ANA M	Accumulator = Accumulator 'AND' [M]	0 • • •	2
ANI byte	Accumulator = Accumulator 'AND' byte	0 • • •	2
ORA r1	Accumulator = Accumulator 'OR' Register r1	0 • • •	1
ORA M	Accumulator = Accumulator 'OR' [M]	0 • • •	2
ORI byte	Accumulator = Accumulator 'OR' byte	0 • • •	2
XRA r1	Accumulator = Accumulator 'EXCLUSIVE OR' Register r1	0 • • •	1
XRA M	Accumulator = Accumulator 'EXCLUSIVE OR' [M]	0 • • •	2
XRI byte	Accumulator = Accumulator 'EXCLUSIVE OR' byte	0 • • •	2
CMP r1	Vergleiche Accumulator mit Register r1	• • • •	1
CMP M	[M] Z=1 : A = (M)	• • • •	2
CPI byte	byte CY=0 : (A) ≥ CY=1 : A < (M)	• • • •	2

Z=0 A ≠ (M)

g. Bef.

		Flags C P Z S	Zyklen
	Rotiere Inhalt vom Accumulator um 1 Stelle nach links	• • • •	1

	Rotiere Inhalt vom Accumulator um 1 Stelle nach rechts	• • • •	1



	Rotiere Inhalt vom Accumulator um 1 Stelle nach links mit Carry	• • • •	1

	Rotiere Inhalt vom Accumulator um 1 Stelle nach rechts mit Carry	• • • •	1

	Bilde 1 er Komplement vom Accumulator	• • • •	1
	Bilde Komplement vom Carry	• • • •	1
	Setze Carry Bit	1 • • •	1

Sprungbefehle

JMP adr	Unbedingter Sprung nach Adresse adr	(PC = adr) • • • •	3
JNZ adr	Springe, wenn ungleich 0	(Z = 0) • • • •	3*)
JZ adr	Springe, wenn gleich 0	(Z = 1) • • • •	3*)
JNC adr	Springe, wenn Carry = 0	(C = 0) • • • •	3*)
JC adr	Springe, wenn Carry = 1	(C = 1) • • • •	3*)
JPO adr	Springe, wenn Parität ungerade	(P = 0) • • • •	3*)
JPE adr	Springe, wenn Parität gerade	(P = 1) • • • •	3*)
JP adr	Springe, wenn positiv	(S = 0) • • • •	3*)
JM adr	Springe, wenn negativ	(S = 1) • • • •	3*)

Unterprogramm Anweisungen

CALL adr	Aufruf der Subroutine mit der Anfangsadresse adr	• • • •	5
CNZ adr	CALL, wenn ungleich 0	(Z = 0) • • • •	3,5**)
CZ adr	CALL, wenn gleich 0	(Z = 1) • • • •	3,5**)
CNC adr	CALL, wenn Carry = 0	(C = 0) • • • •	3,5**)

		Flags C P Z S	Zyklen
CC adr	CALL, wenn Carry = 1	(C = 1) • • • •	3,5**)
CPO adr	CALL, wenn Parität ungerade	(P = 0) • • • •	3,5**)
CPE adr	CALL, wenn Parität gerade	(P = 1) • • • •	3,5**)
CP adr	CALL, wenn positiv	(S = 0) • • • •	3,5**)
CM adr	CALL, wenn negativ	(S = 1) • • • •	3,5**)
RET	Rücksprung aus der Subroutine in das Hauptprogramm	• • • •	3
RNZ	RETURN, wenn ungleich 0	(Z = 0) • • • •	1,3***)
RZ	RETURN, wenn gleich 0	(Z = 1) • • • •	1,3***)
RNC	RETURN, wenn Carry = 0	(C = 0) • • • •	1,3***)
RC	RETURN, wenn Carry = 1	(C = 1) • • • •	1,3***)
RPO	RETURN, wenn Parität ungerade	(P = 0) • • • •	1,3***)
RPE	RETURN, wenn Parität gerade	(P = 1) • • • •	1,3***)
RP	RETURN, wenn positiv	(S = 0) • • • •	1,3***)
RM	RETURN, wenn negativ	(S = 1) • • • •	1,3***)

Interrupt Anweisungen

EI	Enable (ermöglichen) Interrupts	• • • •	1
DI	Disable (verhindere) Interrupts	• • • •	1
RST n	Spezielle Restart-Anweisungen (n = 0, 1, ..., 7)	• • • •	3

Anweisungen für Interrupt-Maske (nur 8085 !)

RIM	Lese Interrupt Maske in den Accumulator	• • • •	1
SIM	Schreibe Interrupt Maske mit dem Inhalt des Accumulators	• • • •	1

Ein-/Ausgabe-Befehle

IN byte	Lese Inhalt des Ports mit Adresse byte in den Accumulator	• • • •	3
OUT byte	Schreibe Inhalt des Accumulators in den Port mit Adresse byte	• • • •	3

Prozessor-Befehle

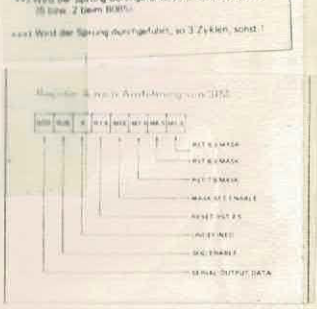
HLT	Hält den Prozessor an	• • • •	1
NOP	Es geschieht nichts	• • • •	1

* unverändert
abhängig vom Resultat verändert
0 immer auf 0 gesetzt
1 immer auf 1 gesetzt

*) Beim 8085: 2 oder 3 Zyklen, je nachdem, ob der Sc... durchgeführt wird.

**) Wird der Sprung durchgeführt, so 5 Zyklen, sonst 3 (8 bzw. 2 beim 8085)

***) Wird der Sprung durchgeführt, so 3 Zyklen, sonst 1



DATA TRANSFER GROUP

Move

MOV	A,A	7F
	A,B	78
	A,C	79
	A,D	7A
	A,E	7B
	A,H	7C
	A,L	7D
	A,M	7E
MOV	B,A	47
	B,B	40
	B,C	41
	B,D	42
	B,E	43
	B,H	44
	B,L	45
	B,M	46
MOV	C,A	4F
	C,B	48
	C,C	49
	C,D	4A
	C,E	4B
	C,H	4C
	C,L	4D
	C,M	4E
MOV	D,A	57
	D,B	50
	D,C	51
	D,D	52
	D,E	53
	D,H	54
	D,L	55
	D,M	56

Move (cont)

MOV	E,A	5F
	E,B	58
	E,C	59
	E,D	5A
	E,E	5B
	E,H	5C
	E,L	5D
	E,M	5E
MOV	H,A	67
	H,B	60
	H,C	61
	H,D	62
	H,E	63
	H,H	64
	H,L	65
	H,M	66
MOV	L,A	6F
	L,B	68
	L,C	69
	L,D	6A
	L,E	6B
	L,H	6C
	L,L	6D
	L,M	6E
MOV	M,A	77
	M,B	70
	M,C	71
	M,D	72
	M,E	73
	M,H	74
	M,L	75

XCHG EB

Move Immediate

MVI	A, byte	3E
	B, byte	06
	C, byte	0E
	D, byte	16
	E, byte	1E
	H, byte	26
	L, byte	2E
	M, byte	36

Load Immediate

LXI	B, dble	01
	D, dble	11
	H, dble	21
	SP, dble	31

Load/Store

LDAX B	0A
LDAX D	1A
LHLD adr	2A
LDA adr	3A
STAX B	02
STAX D	12
SHLD adr	22
STA adr	32

byte = constant, or logical/arithmetic expression that evaluates to an 8-bit data quantity. (Second byte of 2-byte instructions).

dble = constant, or logical/arithmetic expression that evaluates to a 16-bit data quantity. (Second and Third bytes of 3-byte instructions).

adr = 16-bit address (Second and Third bytes of 3-byte instructions).

* = all flags (C, Z, S, P, AC) affected.

** = all flags except CARRY affected; (exception: INX and DCX affect no flags).

† = only CARRY affected.

ARITHMETIC AND LOGICAL GROUP

Add*

ADD	A	87
	B	80
	C	81
	D	82
	E	83
	H	84
	L	85
	M	86
ADC	A	8F
	B	88
	C	89
	D	8A
	E	8B
	H	8C
	L	8D
	M	8E

Subtract*

SUB	A	97
	B	90
	C	91
	D	92
	E	93
	H	94
	L	95
	M	96
SBB	A	9F
	B	98
	C	99
	D	9A
	E	9B
	H	9C
	L	9D
	M	9E

Double Add †

DAD	B	09
	D	19
	H	29
	SP	39

Increment**

INR	A	3C
	B	04
	C	0C
	D	14
	E	1C
	H	24
	L	2C
	M	34
INX	B	03
	D	13
	H	23
	SP	33

Decrement**

DCR	A	3D
	B	05
	C	0D
	D	15
	E	1D
	H	25
	L	2D
	M	35
DCX	B	0B
	D	1B
	H	2B
	SP	3B

Specials

DAA*	27
CMA	2F
STC†	37
CMC†	3F

Rotate †

RLC	07
RRC	0F
RAL	17
RAR	1F

Logical*

ANA	A	A7
	B	A0
	C	A1
	D	A2
	E	A3
	H	A4
	L	A5
	M	A6
XRA	A	AF
	B	A8
	C	A9
	D	AA
	E	AB
	H	AC
	L	AD
	M	AE
ORA	A	B7
	B	B0
	C	B1
	D	B2
	E	B3
	H	B4
	L	B5
	M	B6
CMP	A	BF
	B	B8
	C	B9
	D	BA
	E	BB
	H	BC
	L	BD
	M	BE

Arith & Logical Immediate

ADI byte	C6
ACI byte	CE
SUI byte	D6
SBI byte	DE
ANI byte	E6
XRI byte	EE
ORI byte	F6
CPI byte	FE

BRANCH CONTROL GROUP

Jump

JMP adr	C3
JNZ adr	C2
JZ adr	CA
JNC adr	D2
JC adr	DA
JPO adr	E2
JPE adr	EA
JP adr	F2
JM adr	FA
PCHL	E9

Call

CALL adr	CD
CNZ adr	C4
CZ adr	CC
CNC adr	D4
CC adr	DC
CPO adr	E4
CPE adr	EC
CP adr	F4
CM adr	FC

Return

RET	C9
RNZ	C0
RZ	C8
RNC	D0
RC	D8
RPO	E0
RPE	E8
RP	F0
RM	F8

Restart

RST	0	C7
	1	CF
	2	D7
	3	DF
	4	E7
	5	EF
	6	F7
	7	FF

I/O AND MACHINE CONTROL

Stack Ops

PUSH	B	C5
	D	D5
	H	E5
	PSW	F5
POP	B	C1
	D	D1
	H	E1
	PSW*	F1
XTHL		E3
SPHL		F9

Input/Output

OUT byte	D3
IN byte	DB

Control

DI	F3
EI	FB
NOP	00
HLT	76

New Instructions (8085 Only)

RIM	20
SIM	30

ASSEMBLER REFERENCE

Operators

( )
NUL
LOW, HIGH
*, /, MOD, SHL, SHR
+, —
NOT
AND
OR, XOR

ASSEMBLER REFERENCE (Cont.)

Pseudo Instruction

General:

ORG
END
EQU
SET
DS
DB
DW

Macros:

MACRO
ENDM
LOCAL
REPT
IRP
IRPC
EXITM

Relocation:

ASEG
DSEG
CSEG
PUBLIC
EXTRN
NAME
STKLN
STACK
MEMORY

Conditional Assembly:

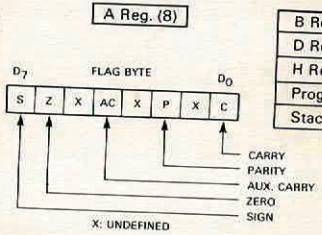
IF
ELSE
ENDIF

Constant Definition

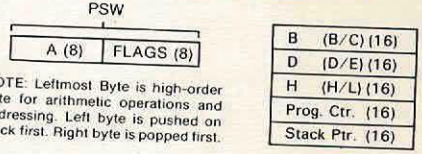
0BDH, 1AH	Hex
105D, 105	Decimal
72O, 72Q	Octal
11011B, 00110B	Binary
'TEST', 'A' 'B'	ASCII

INTEL® 8080/8085 INSTRUCTION SET REFERENCE TABLES

INTERNAL REGISTER ORGANIZATION



REGISTER-PAIR ORGANIZATION



NOTE: Leftmost Byte is high-order byte for arithmetic operations and addressing. Left byte is pushed on stack first. Right byte is popped first.

REGISTER PAIR AND

	Register Pair					
	PSW (A/F)	B (B/C)	D (D/E)	H (H/L)	SP	PC
INX		03	13	23	33	
DCX		0B	1B	2B	3B	
LDAX		0A	1A	7E(1)		
STAX		02	12	77(2)		
LHLD				2A		
SHLD				22		
LXI		01	11	21	31	C3(3)
PCHL						E9
XCHG			EB			
DAD		09	19	29	39	
PUSH	F5	C5	D5	E5		
POP	F1	C1	D1	E1		
XTHL				E3		
SPHL					F9	

Notes: 1. This is MOV A,M. 2. This is MOV M,A. 3. This is JMP.

BRANCH CONTROL GROUP

Jump

JMP adr	C3
JNZ adr	C2
JZ adr	CA
JNC adr	D2
JC adr	DA
JPO adr	E2
JPE adr	EA
JP adr	F2
JM adr	FA
PCHL	E9

Call

CALL adr	CD
CNZ adr	C4
CZ adr	CC
CNC adr	D4
CC adr	DC
CPO adr	E4
CPE adr	EC
CP adr	F4
CM adr	FC

Return

RET	C9
RNZ	C0
RZ	C8
RNC	D0
RC	D8
RPO	E0
RPE	E8
RP	F0
RM	F8

Restart

RST	0	C7
	1	CF
	2	D7
	3	DF
	4	E7
	5	EF
	6	F7
	7	FF

I/O AND MACHINE CONTROL

Stack Ops

PUSH	B	C5
	D	D5
	H	E5
	PSW	F5
POP	B	C1
	D	D1
	H	E1
	PSW*	F1
XTHL		E3
SPHL		F9

Input/Output

OUT byte	D3
IN byte	DB

Control

DI	F3
EI	FB
NOP	00
HLT	76

New Instructions (8085 Only)

RIM	20
SIM	30

ASSEMBLER REFERENCE

Operators

(,)
NUL
LOW, HIGH
*,/, MOD, SHL, SHR
+, —
NOT
AND
OR, XOR

ASSEMBLER REFERENCE (Cont.)

Pseudo Instruction

General:

ORG
END
EQU
SET
DS
DB
DW

Macros:

MACRO
ENDM
LOCAL
REPT
IRP
IRPC
EXITM

Relocation:

ASEG NAME
DSEG STKLN
CSEG STACK
PUBLIC MEMORY
EXTRN

Conditional Assembly:

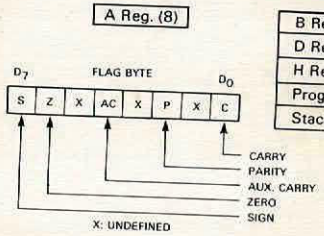
IF
ELSE
ENDIF

Constant Definition

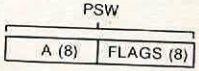
0BDH, 1AH	Hex
105D, 105	Decimal
72O, 72Q	Octal
11011B, 00110B	Binary
'TEST', 'A', 'B'	ASCII

INTEL® 8080/8085 INSTRUCTION SET REFERENCE TABLES

INTERNAL REGISTER ORGANIZATION



REGISTER-PAIR ORGANIZATION



NOTE: Leftmost Byte is high-order byte for arithmetic operations and addressing. Left byte is pushed on stack first. Right byte is popped first.

B	(B/C) (16)
D	(D/E) (16)
H	(H/L) (16)
Prog. Ctr.	(16)
Stack Ptr.	(16)

REGISTER PAIR AND

	Register Pair					
	PSW (A/F)	B (B/C)	D (D/E)	H (H/L)	SP	PC
INX		03	13	23	33	
DCX		0B	1B	2B	3B	
LDAX		0A	1A	7E(1)		
STAX		02	12	77(2)		
LHLD				2A		
SHLD				22		
LXI		01	11	21	31	C3(3)
PCHL						E9
XCHG			EB			
DAD		09	19	29	39	
PUSH	F5	C5	D5	E5		
POP	F1	C1	D1	E1		
XTHL				E3		
SPHL					F9	

Notes: 1. This is MOV A,M. 2. This is MOV M,A. 3. This is JMP.

ASSEMBLER REFERENCE (Cont.)

Pseudo Instruction

General:

ORG
END
EQU
SET
DS
DB
DW

Macros:

MACRO
ENDM
LOCAL
REPT
IRP
IRPC
EXITM

Relocation:

ASEG NAME
DSEG STKLN
CSEG STACK
PUBLIC MEMORY
EXTRN

Conditional Assembly:

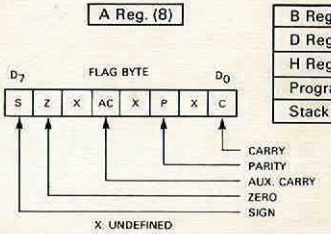
IF
ELSE
ENDIF

Constant Definition

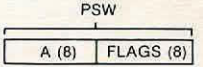
0BDH, 1AH — Hex
105D, 105 — Decimal
72O, 72Q — Octal
11011B, 00110B — Binary
'TEST', 'A', 'B' — ASCII

INTEL® 8080/8085 INSTRUCTION SET REFERENCE TABLES

INTERNAL REGISTER ORGANIZATION



REGISTER-PAIR ORGANIZATION



NOTE: Leftmost Byte is high-order byte for arithmetic operations and addressing. Left byte is pushed on stack first. Right byte is popped first.

B	(B/C) (16)
D	(D/E) (16)
H	(H/L) (16)
Prog. Ctr.	(16)
Stack Ptr.	(16)

BRANCH CONTROL INSTRUCTIONS

Flag Condition	Jump		Call		Return	
Zero=True	JZ	CA	CZ	CC	RZ	C8
Zero=False	JNZ	C2	CNZ	C4	RNZ	C0
Carry=True	JC	DA	CC	DC	RC	D8
Carry=False	JNC	D2	CNC	D4	RNC	D0
Sign=Positive	JP	F2	CP	F4	RP	F0
Sign=Negative	JM	FA	CM	FC	RM	F8
Parity=Even	JPE	EA	CPE	EC	RPE	E8
Parity=Odd	JPO	E2	CPO	E4	RPO	E0
Unconditional	JMP	C3	CALL	CD	RET	C9

ACCUMULATOR OPERATIONS

	Code	Function
XRA A	AF	Clear A and Clear Carry
ORA A	B7	Clear Carry
CMC	3F	Complement Carry
CMA	2F	Complement Accumulator
STC	37	Set Carry
RLC	07	Rotate Left
RRC	0F	Rotate Right
RAL	17	Rotate Left Thru Carry
RAR	1F	Rotate Right Thru Carry
DAA	27	Decimal Adjust Accum.

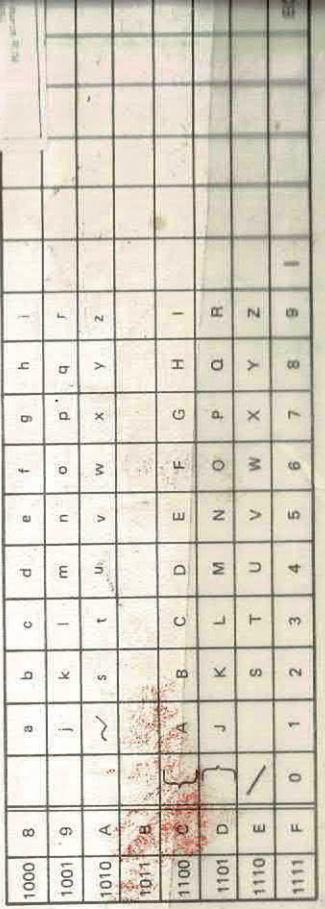
REGISTER PAIR AND STACK OPERATIONS

	Register Pair						
	PSW (A/F)	B (B/C)	D (D/E)	H (H/L)	SP	PC	Function
INX		03	13	23	33		Increment Register Pair
DCX		0B	1B	2B	3B		Decrement Register Pair
LDAX		0A	1A	7E(1)			Load A Indirect (Reg. Pair holds Adrs)
STAX		02	12	77(2)			Store A Indirect (Reg. Pair holds Adrs)
LHLD				2A			Load H/L Direct (Bytes 2 and 3 hold Adrs)
SHLD				22			Store H/L Direct (Bytes 2 and 3 hold Adrs)
LXI		01	11	21	31	C3(3)	Load Reg. Pair Immediate (Bytes 2 and 3 hold immediate data)
PCHL						E9	Load PC with H/L (Branch to Adrs in H/L)
XCHG			EB				Exchange Reg. Pairs D/E and H/L
DAD		09	19	29	39		Add Reg. Pair to H/L
PUSH	F5	C5	D5	E5			Push Reg. Pair on Stack
POP	F1	C1	D1	E1			Pop Reg. Pair off Stack
XTHL				E3			Exchange H/L with Top of Stack
SPHL					F9		Load SP with H/L

Notes: 1. This is MOV A,M. 2. This is MOV M,A. 3. This is JMP.

00	NOP	
01	LXI	B,dble
02	STAX	B
03	INX	B
04	INR	B
05	DCR	B
06	MVI	B,byte
07	RLC	
08	---	
09	DAD	B
0A	LDAX	B
0B	DCX	B
0C	INR	C
0D	DCR	C
0E	MVI	C,byte
0F	RRC	
10	---	
11	LXI	D,dble
12	STAX	D
13	INX	D
14	INR	D
15	DCR	D
16	MVI	D,byte
17	RAL	
18	---	
19	DAD	D
1A	LDAX	D
1B	DCX	D
1C	INR	E
1D	DCR	E
1E	MVI	E,byte
1F	RAR	
20	RIM*	
21	LXI	H,dble
22	SHLD	adr
23	INX	H
24	INR	H
25	DCR	H
26	MVI	H,byte
27	DAA	
28	---	
29	DAD	H
2A	LHLD	adr
2B	DCX	H
2C	INR	L
2D	DCR	L
2E	MVI	L,byte
2F	CMA	
30	SIM*	
31	LXI	SP,dble
32	STA	adr
33	INX	SP
34	INR	M
35	DCR	M
36	MVI	M,byte
37	STC	
38	---	
39	DAD	SP
3A	LDA	adr
3B	DCX	SP
3C	INR	A
3D	DCR	A
3E	MVI	A,byte
3F	CMC	
40	MOV	B,B
41	MOV	B,C
42	MOV	B,D
43	MOV	B,E
44	MOV	B,H
45	MOV	B,L
46	MOV	B,M
47	MOV	B,A
48	MOV	C,B
49	MOV	C,C
4A	MOV	C,D
4B	MOV	C,E
4C	MOV	C,H
4D	MOV	C,L
4E	MOV	C,M
4F	MOV	C,A
50	MOV	D,B
51	MOV	D,C
52	MOV	D,D
53	MOV	D,E
54	MOV	D,H
55	MOV	D,L
56	MOV	D,M
57	MOV	D,A
58	MOV	E,B
59	MOV	E,C
5A	MOV	E,D
5B	MOV	E,E
5C	MOV	E,H
5D	MOV	E,L
5E	MOV	E,M
5F	MOV	E,A
60	MOV	H,B
61	MOV	H,C
62	MOV	H,D
63	MOV	H,E
64	MOV	H,H
65	MOV	H,L
66	MOV	H,M
67	MOV	H,A
68	MOV	L,B
69	MOV	L,C
6A	MOV	L,D
6B	MOV	L,E
6C	MOV	L,H
6D	MOV	L,L
6E	MOV	L,M
6F	MOV	L,A
70	MOV	M,B
71	MOV	M,C
72	MOV	M,D
73	MOV	M,E
74	MOV	M,H
75	MOV	M,L
76	HLT	
77	MOV	M,A
78	MOV	A,B
79	MOV	A,C
7A	MOV	A,D
7B	MOV	A,E
7C	MOV	A,H
7D	MOV	A,L
7E	MOV	A,M
7F	MOV	A,A
80	ADD	B

*8085 Only.



9010

NCR

NCR I-8100 SERIES 8140 POCKET REFERENCE

SECOND EDITION

8" Floppy