E L Z E T 8 0

Interface zum Anschluß von PHILIPS Mini-Digitalrecordern (MDCR)

ELZET 80

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TECHNISCHE BESCHREIBUNG ELZET'-80 MINI-DCR CONTROLLER

Die DCR Controller Platine des ELZET-80 Systems enhält als Kernstück die neu auf dem Markt befindliche Z80-UART "DART". Der Baustein enthält zwei interruptfähige serielle Übertragungskanäle und eine Anzahl frei programmierbarer Ein- und Ausgänge pro Kanal. Sie gestatten eine vollständige Steuerung von zwei Mini-DCR's mit einem Minimum an komplexen Bausteinen.

Die Controller-Platine ist voll gepuffert. Sie belastet den CPU-Bus mit nur einer LS-Last.
Der Sendetakt wird für beide Schnittstellen getrennt mit einem CTC-Baustein erzeugt.
Den Empfangsclock erzeugt das Laufwerk. Somit ist die Datenqualität von Gleichlaufschwankungen des Laufwerkes weitestgehend unabhängig.

Übertragungsform: Serielle Datenübertragung
6000-9600 BIT'S
Remote Control über 2 programmierbare Ausgänge
Rückmeldung über 3 Eingänge des "DART"

Ausgänge	DTR	RTS	
	H	H	Laufwerk disabled
	L	H	Rewind
	H	L	Read Data
	L	L	Write Data

Die Bits RTS/DTR müssen im Writeregister 5 Invers zum gewünschten Ausgangssignal gesetzt werden.

Eingänge	RI	Meldung	Bet (begin/end of Tape)
	CTS		WEN (write enabled)
	DCD		CIP (Cassette in Position)

Alle Meldungen vom Laufwerk sind Activ Low.

Der Status dieser Eingänge kann durch lesen des Read Registers 0 überprüft werden.

Der Anschluß der Laufwerke erfolgt über einen 26 poligen Pfostenstecker. Mittels einer umsteckbaren Brücke können die Treiber Bausteine 12V vom der DCR Versorgung oder vom Bus erha lten. Verbindet man alle drei Pfosten miteinander wird auch das Laufwerk vom Bus versorgt.

In das Write Register 1 muß beim schreiben immer der Wait/Ready-Ausgang auf Ready - Funktion programmiert werden.

Die Aufzeichnungsform der Daten beim DCR-Laufwerk ist eine "Richtungstaktschrift". Das heißt, die Bits werden durch die Richtung einer Signalflanke zu einem bestimmten Zeitpunkt dargestellt.
Diese Richtungstaktschrift wird durch die Exor-Verknüpfung des Daten Wortes und des Taktes, der die Übertragungsgeschwindigkeit bestimmt, realisiert. Vorraussetzung ist ein symmetrischer Takt. Dieser wird durch teilen der doppelten Baudrate, mittels eines Flipflops, erzeugt. Die Baudrate wird mit einem Timer Baustein erzeugt. (CTC)

Beim lesen der Daten generiert das DCR Laufwerk den Lesetakt selber. Der Lesetakt wird an den Clockeingang und der Datenausgang des DCR auf den D- Eingang eines D-Flipflops gelegt.
Mit der negativen Flanke des Clocks übernimmt das Flipflop das Datembit. Mit der positiven Flanke wird das Bit in die Schnittstelle eingelesen. Es findet somit eine Zwischenspeicherung des Datenbits, das die Übertragungssicherheit erheblich erhöht.

Einstellung der Portadresse für ELZET III MDCR Monitor Vers. 3.4

Die Portadresse wird von der Software mit 48 - 4F(H) angenommen

Dazu ist der 4p DIL-Schalter wie folgt zu stellen :

A4 = ON / A5 = ON / A6 = OFF / A7 = ON

Der Jumper A3 rechts über dem DIL-Schalter ist auf H zu stellen.

Steckerbelegung des 26-poligen Pfostensteckers zu den Laufwerken :
Bitte beachten Sie, daß der untere Teil des Steckers für das erste Laufwerk (Laufwerk Nummer Ø) belegt ist. Pins 8 bis 19 also für das Laufwerk Ø, pins 1-7 und 20-26 für Laufwerk 1 !

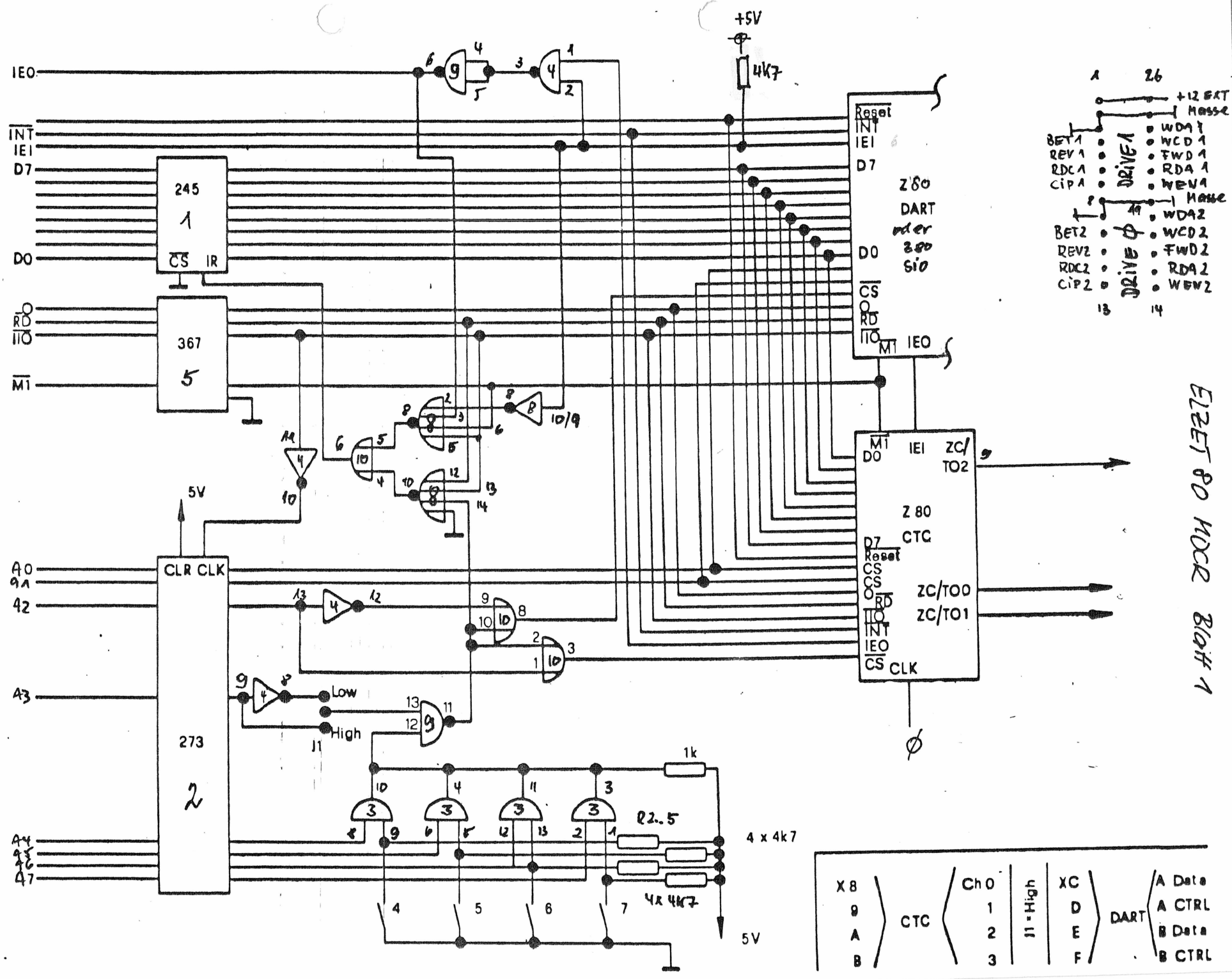
Die von uns als Monitor ELZET III Vers. 3.4 angebotene Betriebssoftware verlangt für die korrekte Funktion den Betrieb des Video-Terminals mit mindestens 9600 Baud !
Durch die Ausgabe von Zeichen zum Bildschirm während des Lesens oder Schreibens wird die Übertragung unterbrochen, wenn das Video-Terminal das letzte Zeichen noch nicht komplett ausgegeben hat und ein neues anliegt.

Stückliste ELZET 80 Mini-DCR

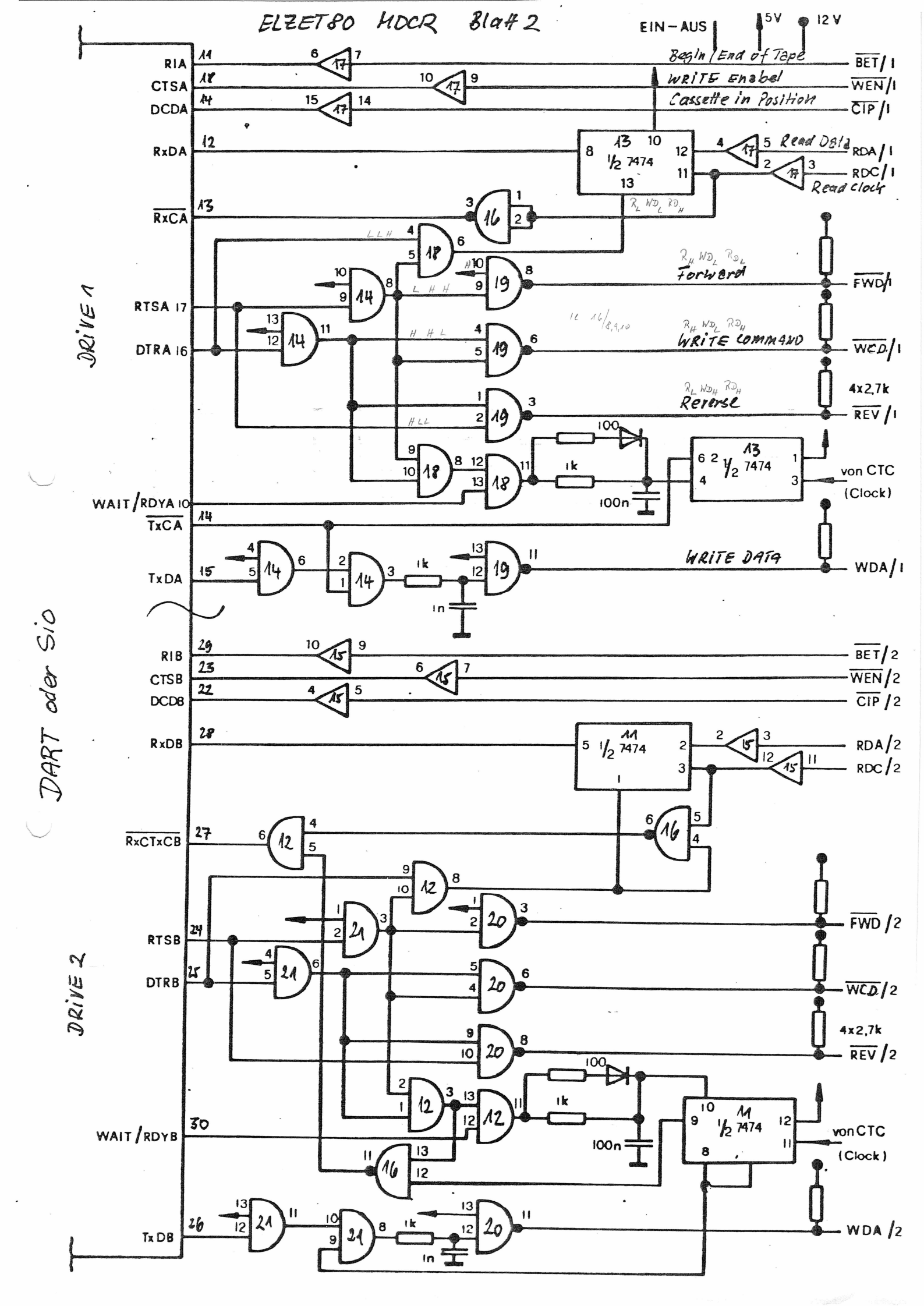
IC 1	74LS245
IC 2	74LS273
IC 3	74LS266
IC 4	74LS04
IC 5	74LS367
IC 6	Z80 CTC
IC 7	Z80 DART oder SIO
IC 8	7423
IC 9,16	74LS00
IC 10	74LS32
IC 11	74LS74
IC 12,18	74LS08
IC 13	74LS74
IC 14	74LS86
IC 15,17	CD4050
IC 19,20	74LS26
IC 21	74LS86

R 1	680Ω	R 18 (unterhalb CTC),
R 2-5	4,7kΩ	nur notwendig, wenn
R 6,8	100Ω	Interrupt-Prioritäts-
R 7,9,		kette nicht korrekt
18,19	1kΩ	geschlossen ist :
R 10-17	2,7kΩ	4,7 kΩ

D 1	1N4001-4007
D 2,3	1N4148
C 1-3	47µF/16V Elko st.
C 4,5	100nF
C 6,7	1nF
C 8	22µF/16V Elko st.



ELZET 80 MICRO BLOCK 1


ELZET80 MDCR Blatt 2
EIN – AUS
5V
12 V
Begin / End of Tape
WRITE Enabel
Cassette in Position
Read Data
Read clock
Forward
WRITE COMMAND
Reverse
WRITE DATA
4x2,7k
100n
1k
1n
von CTC (Clock)
DRIVE 1
DRIVE 2
DART oder SIO
RIA
CTSA
DCDA
RxDA
RxCA
RTSA 17
DTRA 16
WAIT/RDYA 10
TxCA
TxDA
RIB
CTSB
DCDB
RxDB
RxCTxCB
RTSB
DTRB
WAIT/RDYB
TxDB
BET/1
WEN/1
CIP/1
RDA/1
RDC/1
FWD/1
WCD/1
REV/1
WDA/1
BET/2
WEN/2
CIP/2
RDA/2
RDC/2
FWD/2
WCD/2
REV/2
WDA/2
7474

I. General

1. Introduction

This manual provides the description, timing diagram, interfacing signals as well as operating and maintenance instructions for the Philips mini-digital cassette recorder.
The Philips Mini-DCR has been specially designed for O.E.M.'s and users that need a fast and low-cost serial memory device for data storage and interchange.
The Mini-DCR is available in either a read-only or read-and-write version.
The recorder uses the Philips mini-cassettes, certified for freedom from drop-outs.

The whole system is based on Philips' extensive know-how gained in many years experience of digital cassette recording systems and their applications.
Advantages of economy, cassette convenience and high performance have made this technique internationally accepted and Philips quality and reliability have made them a major O.E.M. supplier of this type of equipment.

The Philips Mini-DCR is an ideal unit for micro-processor based systems, terminals, mini-computers and scientific calculators to be used in program loading, memory back-up and data capture applications.

2. Technical specification

Number of heads	:	two; a read/write head and an erase head
Recording head	:	single gap, single track, half width, read/write head
Number of tracks	:	two; A-side and B-side
Recording method	:	phase encoding character/bit serial
Tape length	:	36 m
Data transfer rate	:	6000 bits per second
Recording density	:	300 - 500 bpi (12-20 b/mm)
Irrecoverable error rate	:	1 in 10^9 bits
Tape transport	:	single motor hub driven 360 rpm ± 5%
Tape speed	:	12 - 20 ips (300 - 500 mm/sec.)
Read/write time	:	95 sec. for full tape length
Start time read/write	:	< 100 msec.
Stop time read/write	:	30 - 100 msec.
Start distance	:	0.6 - 2.0 inch (15 - 50 mm)
Stop distance	:	0.2 - 1.0 inch (5 - 25 mm)
Rewind time	:	< 95 sec.
Data capacity	:	64k octads per track
Medium	:	Philips 3.81 mm mini cassette certified for freedom of drop-outs

Electronics
Read/write electronics, tape transport

Control logic	:	one printed circuit board
Signal interface	:	the signal interface is a MOS-compatible (HEF 4000p series) interface
Signal levels/output signals	:	logic "1" Vs minus 0.5 V logic "0" < 0.5 V
Signal levels/input signals	:	logic "1" 8 V–Vs logic "0" < 3 V
Power interface	:	DC-power Vs = 12 volt ± 5%
Power load	:	400 mA peak (100 msec.) 120 mA nominal 30 mA stand-by
Thermal dissipation	:	1.4 Watt nominal
Electrical connections	:	via Amp. connector. 14 Pins cis serie Amp. code 164334 (13 pins) Housing 1-163690-3

Environmental conditions

Operating temperature range:		+5°C to +55°C
Thermal shock	:	< 11°C per hour
Relative humidity	:	10% - 90% (no condensation)
Air pressure	:	780 - 1100 mbar
Vibration (IEC 68-2-6)	:	5 - 200 Hz at 1g curve
Heat radiation	:	direct sunlight radiation on the cassette drive is not allowed
Physical dimensions	:	see fig. 1
Weight of Mini-DCR	:	about 400 grams

3. Type-numbers

8920 405 10101	:	basic read-only unit (MCR 210)
8920 405 10201	:	basic read and write unit (MCR 220)
8920 405 10301	:	MCR 210 with front cover (see fig. 1)
8920 405 10401	:	MCR 220 with front cover (see fig. 1)
8920 405 10601	:	MCR 220 with front cover and write enable switch
8920 440 10101	:	certified mini-cassette in plastic cover

II Use of the Mini-DCR

1. Interfacing

The plug connections are given in fig. 6/7 and the interface signals and their function are listed in the following section. The timing diagram in fig. 10 gives information about the various interface signals and commands.

– To guard against any fire hazard the following measures should be taken:
A. insert a fuse 0.5 A in the positive leads of the 12 Volt supply.
B. the supply leads and earth leads must each have a minimum cross-section of 0.38 mm^2.
– It is recommended that cassettes be entirely (re-)wound before they are removed from the recorder.
This prevents the tape from being touched by the fingers during loading and unloading.
Formation of unwanted loops is also avoided.
– If the direction of the tape movement is changed the start time will be about 50 msec. longer.
The start distance will be between 30 and 65 mm.
– To prevent false writing the unit shall not be switched-on or -off in case a cassette has been loaded unless the rise/fall time is < 1 µsec.
– Each mini-cassette can be equipped with a write-enable plug in order to prevent writing on a recorded tape.
The position of the write-enable plug determines wether writing is enabled on track 1 or 2 (see fig. 3).

2. Operating instructions

Since the Mini-DCR is intended for use by O.E.M. customers, operation of the device will depend upon individual system requirements.

Cassette loading is accomplished by depressing the button adjacent to the cassette cover and inserting the mini-cassette, open end first, into the cassette cover and closing the cover.

3. Operators maintenance

The only maintenance required for the user is cleaning of the read/write head every working week or 100 hours.
Use cotton wool buds slightly wetted with ethanol.

4. Survey of interface signals

Name	Stands for:	Cat.	Description:	If "0"	If "1"
$\overline{WDA}$	Write data	D	Input channel of the write amplifier accepting information in digital form to be recorded on tape (6000 Hz ± 1%)	PE-encoded data "0" is a neg. going signal. Data "1" is a positive going signal. In the gaps signal $\overline{WDA}$ is at high level	
$\overline{BET}$	Begin/end of tape	S	Indicates whether begin of tape or end of tape has been detected.	Begin or end of tape had been detected.	
$\overline{WCD}$	Write command	C	Enables information entering via WDA-line. Also causes erasure of the tape.	Gate is open.	Gate is closed.
$\overline{REV}$	Reverse	C	Causes tape transport in the reverse direction.	Initiates tape transport.	Stops tape transport.
$\overline{FWD}$	Forward	C	Causes tape transport in forward direction.	Initiates tape transport.	Stops tape transport.
RDC	Read clock	D	Separately generated clock signal to strobe read data	Positive going edge should be used to clock read-data.	
$\overline{RDA}$	Read data	D	Output channel of the read amplifier, supplies digital data that has been read from the tape.	PE-encoded data "0" is a negative going signal. Data "1" is a positive going signal. In the gaps signal $\overline{RDA}$ is at high level.	
$\overline{CIP}$	Cassette in position	S	Indicates that a cassette is in position and the door has been closed.	Cassette is present.	No cassette.
$\overline{WEN}$	Write enable	S	Indicates whether or not a write enable plug is present in the cassette. (file protection)	Allows writing on tape (plug is present).	Write action prohibited

Note: C = control signal; D = data signal; S = status signal.

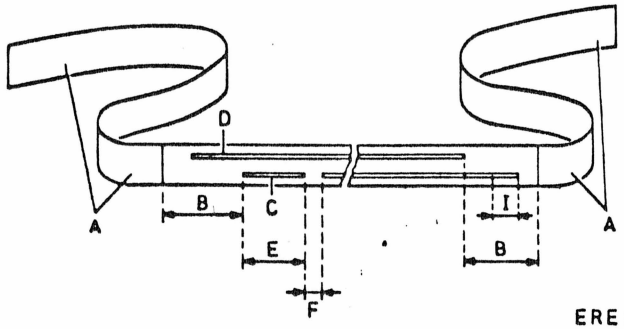
1. Technical Description

Cassette Composition
Figure 2 shows the physical composition of the tape.
Figure 4 shows the composition of the data blocks.

Gaps
Initial gaps, interblock gaps and end of data gaps are all erased to the same polarity.
This polarity is called the reference polarity.
For this purpose the $\overline{\text{WDA}}$-line should remain high.

Phase encoding (see fig. 5,
Data bits (i.e. "zeroes" and "ones") are written as flux transitions such that a "1" bit causes a transition to the reference polarity and a "0" bit causes a transition opposite to the reference polarity.
When successive "1" or "0" bits are written, it is necessary to insert extra transitions between the data bits to establish the correct polarity. These transitions are known as phase flux transitions.
Note: All datablocks have to start with a pre-amble-character to synchronise the read electronics (see fig. 4).

Write Data
The phase encoded (PE) $\overline{\text{WDA}}$-signal is input at 15 IC1 and appears in-phase at 11 IC1 and anti-phase at 9 IC1.



A – Tape leader.
B – Initial gap.
C – Track 1.
D – Track 2.
E – Data block.
F – Interblock gap.
I – End of block gap.

Fig. 2. Mini-DCR – Physical Composition of Tape.

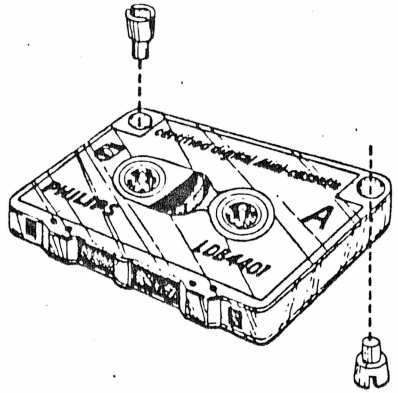


Fig. 3. Mini-DCR – Physical Composition of the Mini-Cassette

These two signals are applied across the read/write head when the $\overline{\text{WCD}}$ signal 9 IC6 is LOW and the WEN switch closed (8, 9 IC9-high). Enabling IC1 (4 IC1-low) also causes a low level; from 2 IC1, to be fed via R56 to the base of TS6 causing current to flow through the erase head.

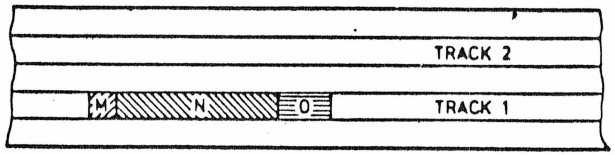
Read Data
The read signal from the read/write head is amplified via 2, 1 IC2 and applied to the pulse-shaper and rectifier ciircuit. The negative pulses inverted and amplified via 6, 7 IC2 and recombined with the amplified positive pulses from 8 IC2. Further shaping and squaring is carried out via TS7 and IC6.

The square-wave read data signal is phase-coded via 3, 1 IC7 and appears at output pin 12 ($\overline{\text{RDA}}$).
The read clock signal is derived from the read data signal via 2, 3 IC3 and appears at output pin 11 (RDC) to indicate a valid $\overline{\text{RDA}}$ output when positive.

Motor Control Logic
A low signal on either the $\overline{\text{FWD}}$ or $\overline{\text{REV}}$ inputs will cause switch "on" of TS2, TS5 or TS3, TS4 respectively.
The amount of current flowing through these transistors (and the motor) is controlled by TS1.
TS1 is driven by the servo loop formed by the motor, the tacho generator and IC's 4, 5 and 6.

BET and Tape Stopped Retector
A sample of the positive output from 8 IC5 is fed to 3 IC5 to hold the BET line high; should the tape jam or the motor stop, the output 8 IC5 goes negative causing a low on the $\overline{\text{BET}}$ line.

Clear Logic
When both $\overline{\text{REV}}$ and $\overline{\text{FWD}}$ lines are high the CLEAR signal output ate 11 IC9 goes high causing the following:
i) $\overline{\text{BET}}$ line high via 2 IC5.
ii) TS1 cut-off via 12 IC5.
iii) Preset of the RDA and RDC flip-flops IC7.



M – preamble = 10101010.
N – data undefined block length least significant bit is read and written first.
O – CRC character 16 bits.

Fig. 4. Mini-DCR – Data Block Composition. ERE 6380

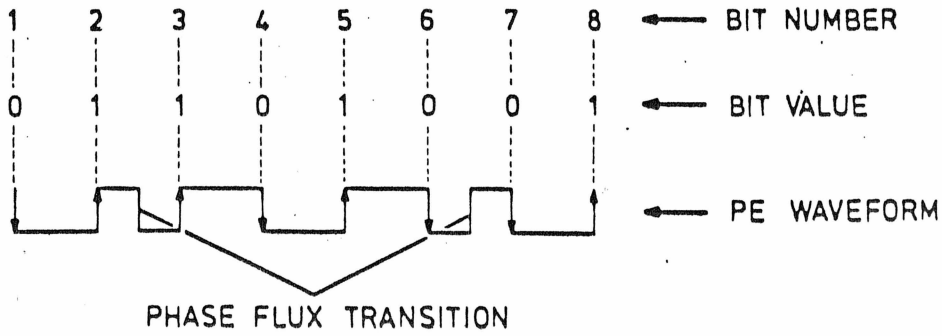
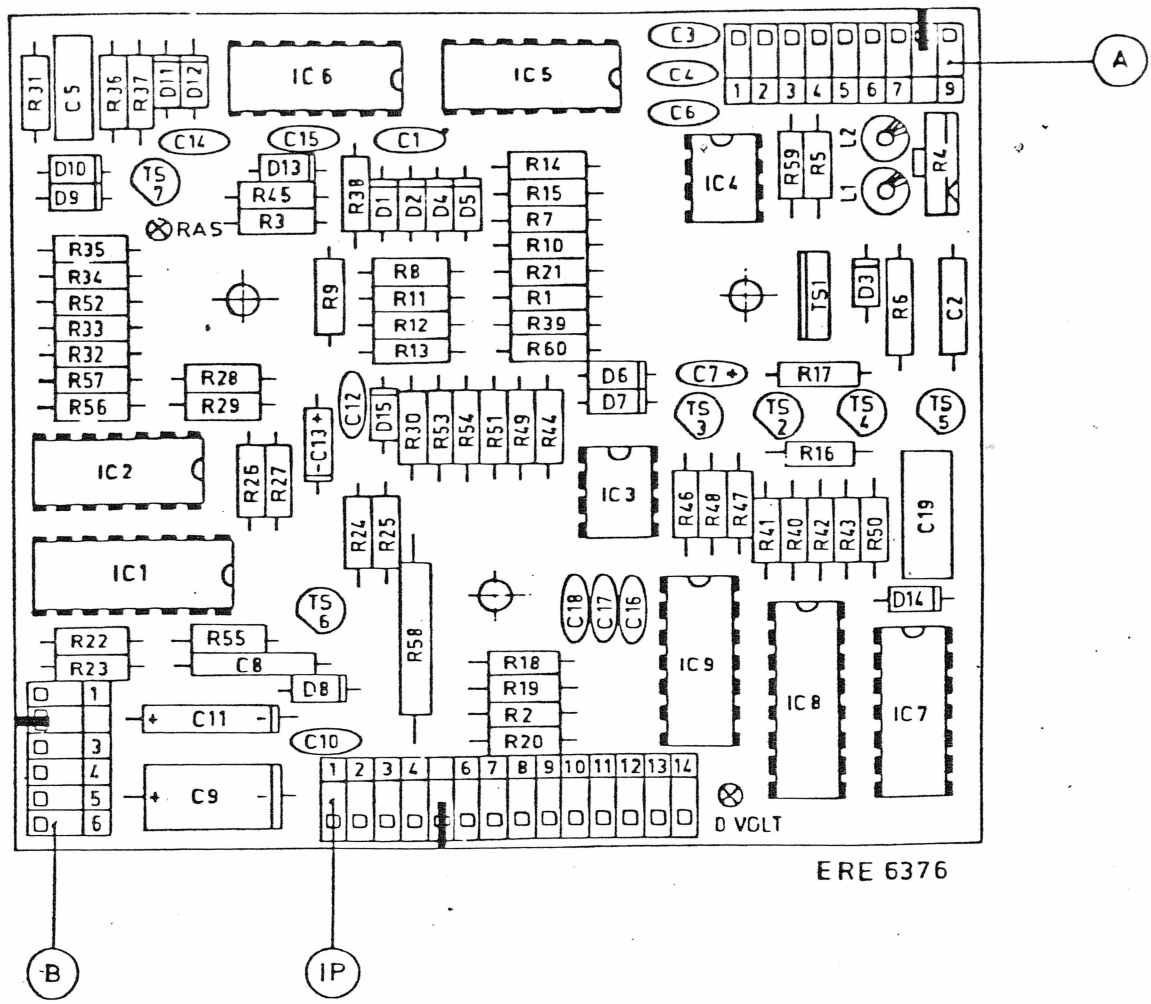


Fig. 5. Mini-DCR – Phase Encoded Write Data. ERE 6383

Fig. 10. Mini-DCR – PCB Layout.



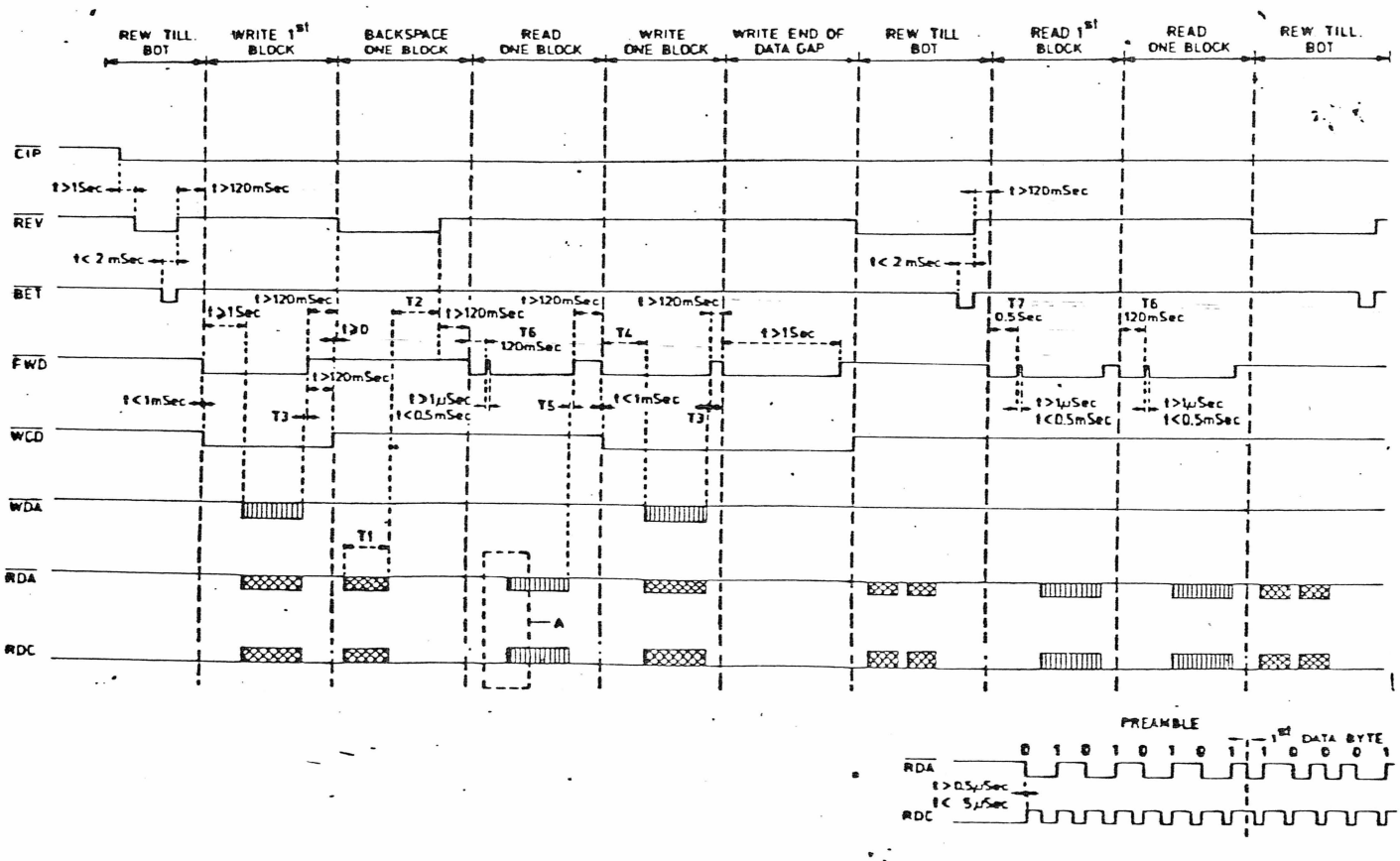


Fig. 11. Mini-DCR – Timing Diagram.

2. Timing Diagram

T1: The length depends on selected block-length and the relative position on the tape.
T2-T3-T4-T5: Depend on selected block-length, the total number of blocks and the start/stop, distances/times.
T6-T7: The pulses on the $\overline{FWD}$ line are necessary for clearing the Read Electronics.

How to use tape capacity efficiently
1. Required tape capacity: 32k-bytes per track (128 blocks of 256 bytes each).
T2 = 1/3 T1; T3 = 40 m sec.;
T4 = 250m sec.; T5 = 0. In case of re-write one block T4 = 350m sec.
2. Required tape capacity: 24k-bytes per track (96 blocks of 256 bytes each).
T2 = 198m sec.; T3 = 40m sec.;
T4 = 450m sec.; T5 = 0.
3. Required tape capacity: 40k-bytes per track (40 blocks of 1024 bytes each).
T2 = 198 m sec.; T3 = 40m sec.;
T4 = 450 m sec.; T5 = 0.
4. Required tape capacity: 64k-bytes per track (1 block of 64k-bytes).
T2 = Rewind time till BOT; T3 = time to write end of data gap; T4 is not applicable.

Remarks
– During a continuous write operation (no backspace or control-read) T3 = 0m sec. in order to obtain optimum data capacity.
– Repeated updating of a data-block positioned between two other blocks, may cause overwriting of the first part of the next data block.
– The pre-amble is used to synchronise the Read-clock (see detail A of the timing diagram).
– Read DATA is TRUE at the positive pulse edge of the signal Read clock.
– To read two or more blocks of data continuously it is necessary to reset Read clock in the inter-block gaps. This can be achieved by a pulse on the $\overline{FWD}$-line of:
$1\,\mu s < T < 0.5$m sec.
– During Read operation signal $\overline{WDA}$ may not change level, because this causes cross-talk on $\overline{RDA}$.
– Signal $\overline{BET}$ indicates both begin and end of tape.
– In case of rewriting blocks, T4 shall be at least 100 msec. longer as indicated.

3. Maintenance

The only maintenance required for the Mini-DCR is cleaning of the read/write head every week or 100 working hours.

4. Adjustments

Electronic
1. The motor speed can be adjusted via R4 to give a mean tacho frequency of 1075 Hz (i.e. approximately 45 seconds after starting forward with a cassette loaded).

Mechanical
1. The mechanical forward/reverse switching element has two stop-screws that should be adjusted individually to give minimum motor current in either direction.

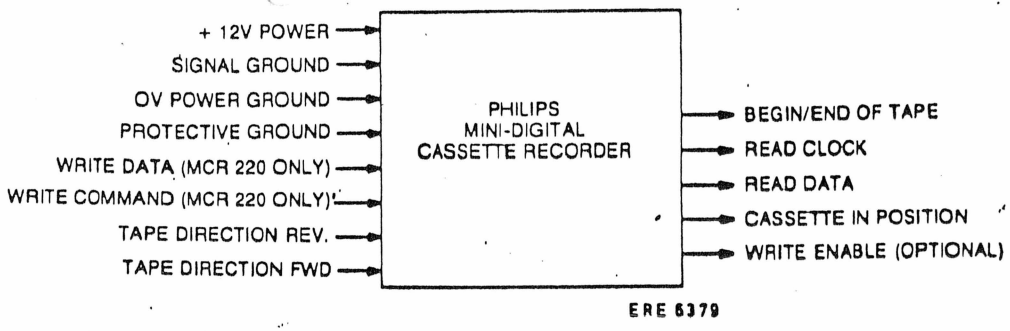
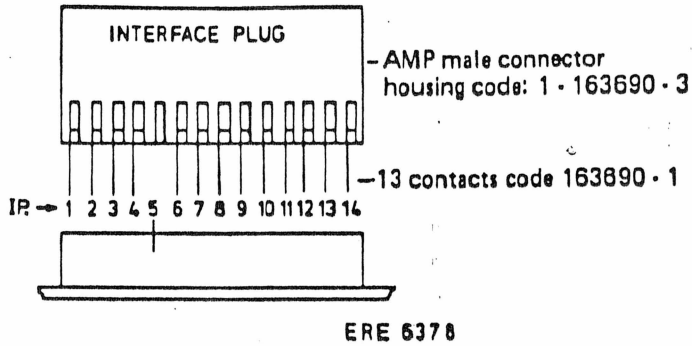


Fig. 6. Mini-DCR – Interface Diagram.



Pin No.	Signal
1	12V
2	OV (Signal Ground)
3	OV (Power)
4	Earth (Protective Ground)
6	$\overline{WDA}$
7	$\overline{BET}$
8	$\overline{WCD}$
9	$\overline{REV}$
10	$\overline{FWD}$
11	$\overline{RDC}$
12	$\overline{RDA}$
13	$\overline{CIP}$
14	$\overline{WEN}$

Fig. 7. Mini-DCR – Interface Connector.

Data subject to change without notice.

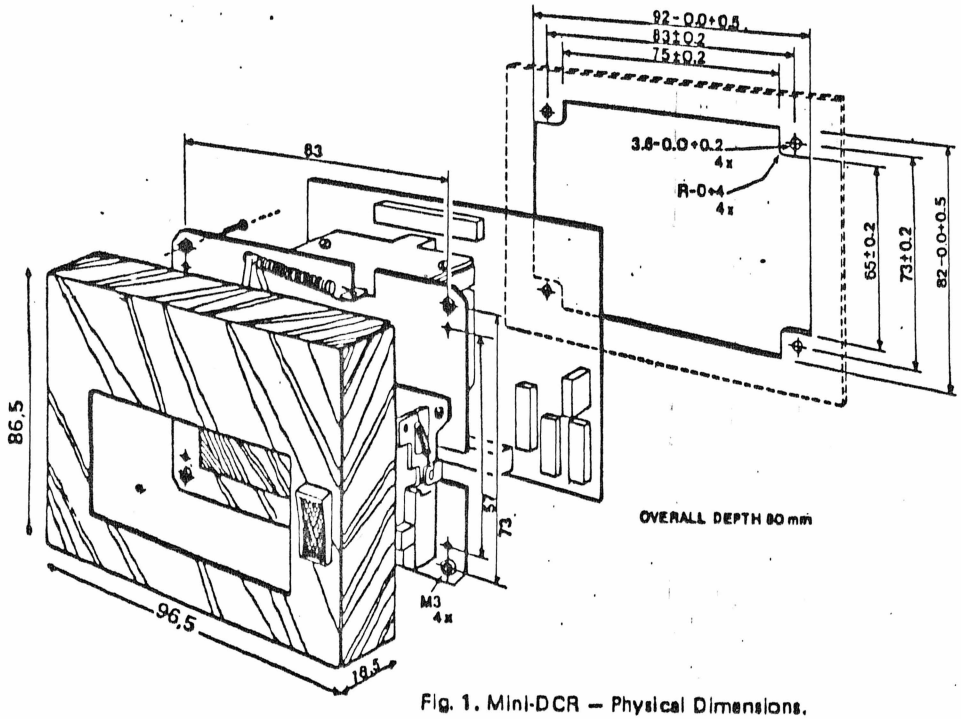


Fig. 1. Mini-DCR – Physical Dimensions.

ERRATA

Page 4: Tape transport: 338 rpm ± 5%
Tape speed: 10.6-18 ips
(270-450 mm/s)
Stop time read/write: 30-120 ms.

Page 5: Electrical connections: code nr.
for pin: 163691-1.
Type: nrs. 8920 405 10401
MDCR with WEN switch
Note: 8920 405 10601
is the standard MDCR
version
8920 405 10602
is the code nr. for a box
containing 20 standard
MDCR units.

Page 11: Interface plug: code nr. for the
AMP-contacts 163691-1

Page 13: In the circuit diagram input signal
at IP-6 has to be $\overline{\text{WDA}}$

- This document can be subject to change
without prior notice -

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Telex 931473 laden
Volksbank Osnabrück
(BLZ 26590025)
Konto 10103711

ELZET 80 DAS UNIVERSELLE MIKROCOMPUTERSYSTEM

Ihr Zeichen Your ref.	Ihr Schreiben vom Your letter dated	Unser Zeichen Our ref.	Datum Date

Sehr geehrter MDCR-Kunde,

Betr.:
Re.: im Rahmen der Software-Wartung bieten wir Ihnen heute den Austausch der Mini-DCR-Systemsoftware an.

Insbesondere bei schlecht justierten Laufwerken erscheint die Fehlermeldung "NO SYNC DETECTED" auch dann, wenn noch eine Datei an der Abbruchstelle zu lesen wäre. Zwar kann mit einem neuen Anlauf der Lesevorgang dann durchgeführt werden, aber der Effekt wirkt natürlich störend und kann wie folgt behoben werden :

a) Bootprogramm:
Kompletter Austausch erforderlich, bitte Cassette einschicken

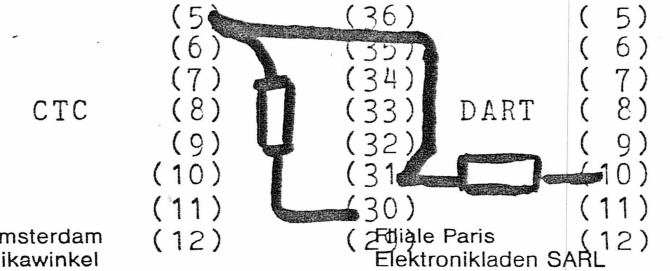
b) Monitor:
Speicherstelle EC79 von "CD F4EB" auf "CD 12EA" ändern. Wenn kein Eprom-Programmierer zur Verfügung steht, bitte entsprechendes Eprom zusammen mit Cassette an uns einsenden.

c) Hardware:
Zwei Anschlüsse des DART/der SIO müssen mit zwei Widerständen 1k nach Masse gezogen werden. Es sind dies die Pins 10 und 30. Masse ist z.B. an 31 oder an 5 des CTC. Die Handskizze unten verdeutlicht die günstigste Plazierung der Widerstände. Überprüfen Sie bitte bei der Gelegenheit auch, ob der IEI-Pullup 4,7kOhm, der nicht auf dem Bestückungsdruck ist, eingelötet wurde. Unter dem CTC befinden sich in entsprechendem Abstand zwei unbezeichnete Lötaugen neben der Bezeichnung "DCR-CONTROLLER".

Die Neuprogrammierung von a) und b) erfolgt bei Einsendung der Datenträger kostenlos, wünschen Sie, daß wir auch die Hardwaremodifikation vornehmen, so müssen wir unseren üblichen Stundensatz für Reparaturen berechnen.

Mit freundlichen Grüßen

ELEKTRONIKLADEN



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MDCR

	a	c
1	+5V	+5V
2	D5	D0
3	D6	D7
4	D3	D2
5	D4	A0
6	A2	A3
7	A4	A1
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	10	ws	BET	2	
18		gr	WDA	2	
	9	vi	Masse		
19		bl	Masse		
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	5	ws	REV	1	
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