G E N I E III

EG 3200

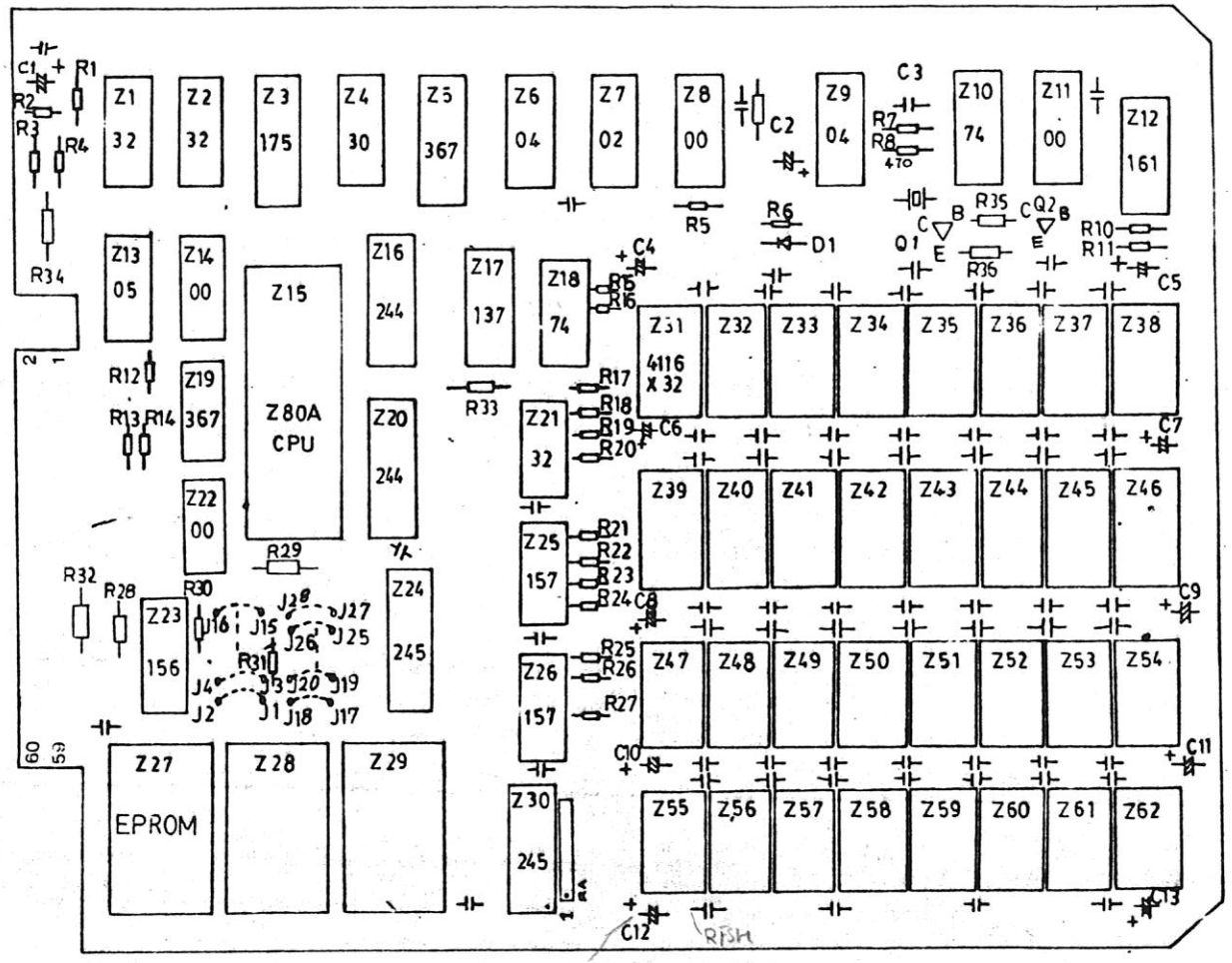
SCHEMATICS

AUGUST, 1982.

EACA COMPUTER LTD.

MARKETING

3 AUG 1982

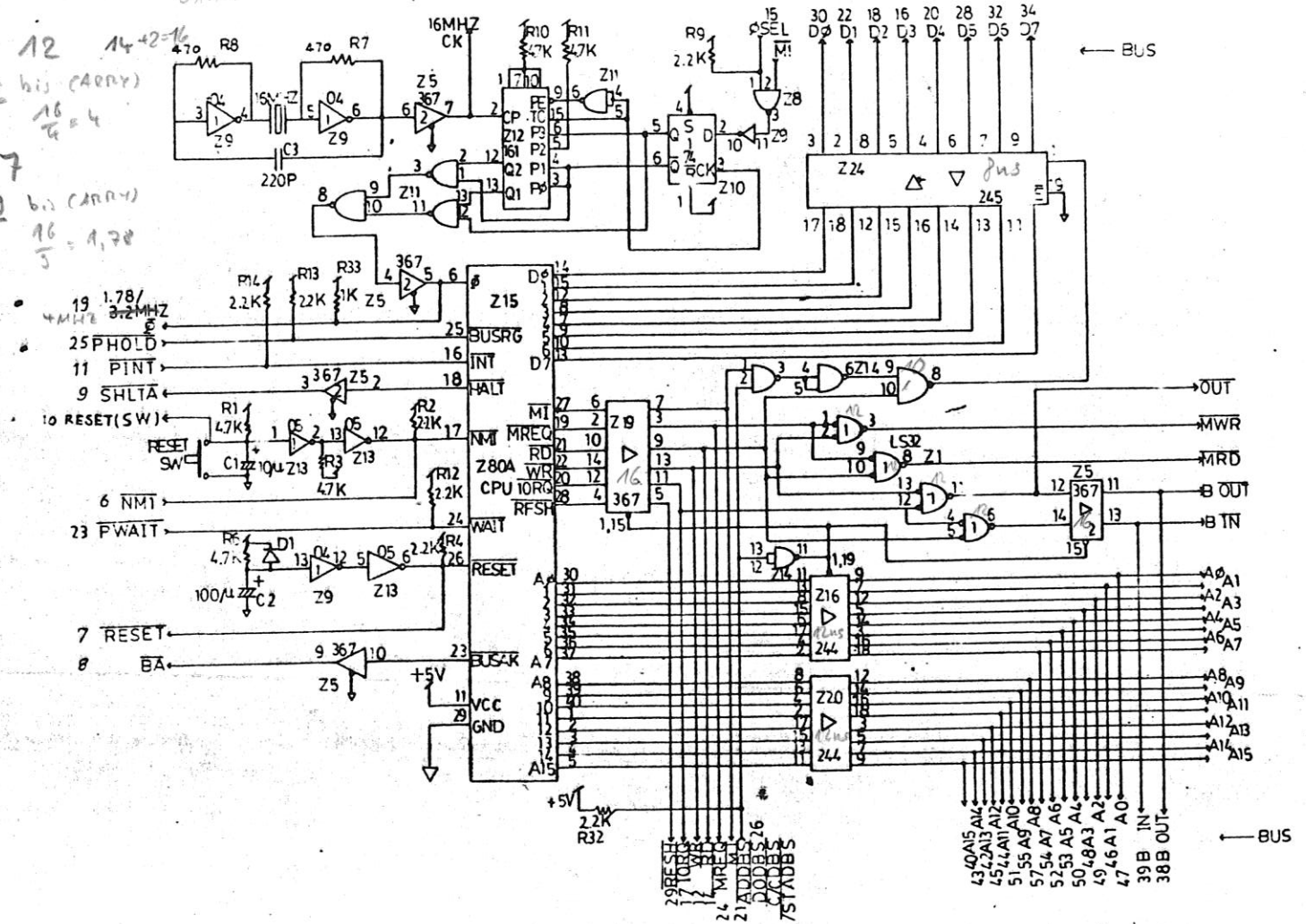


A7

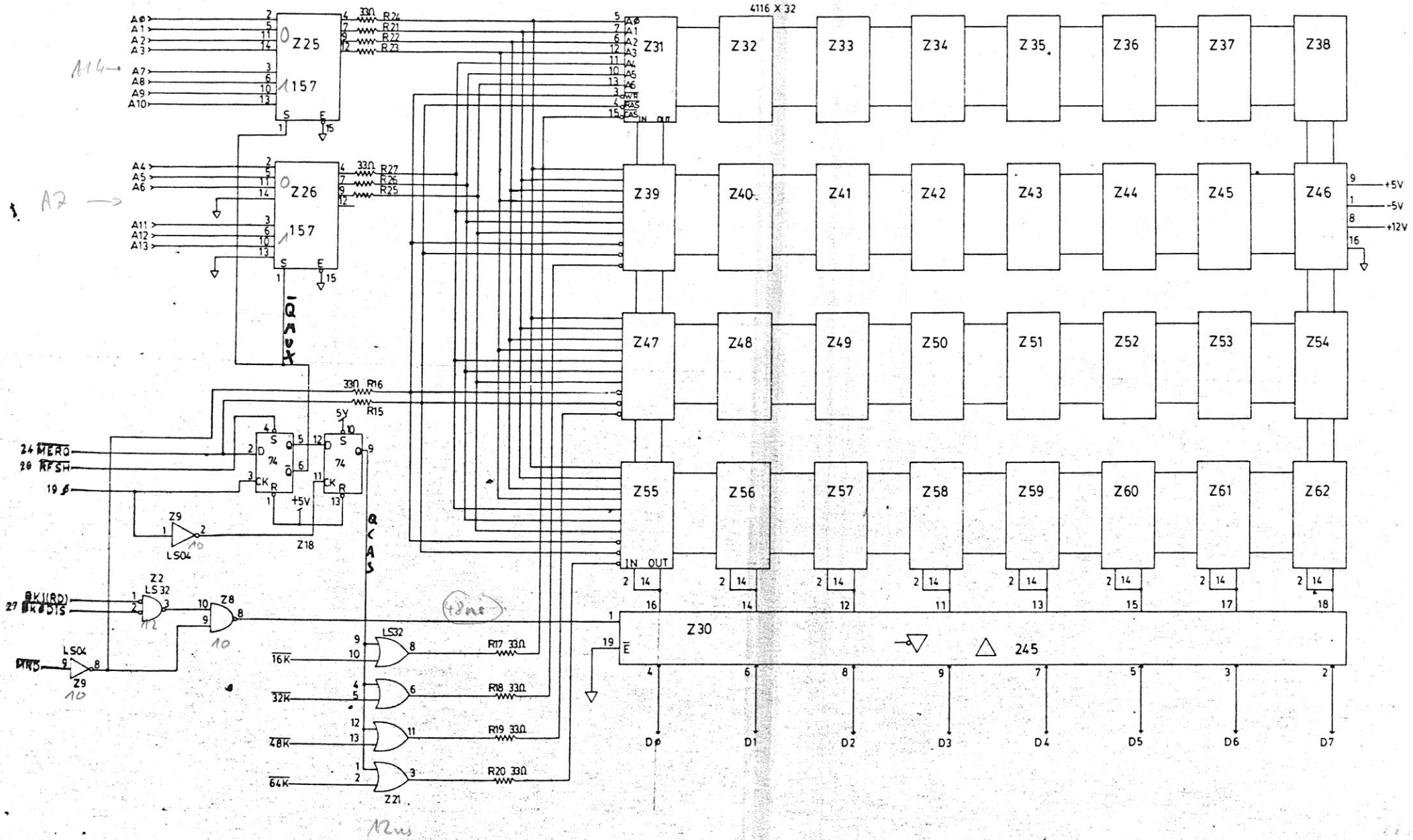
GENIE III CPU BOARD

MARKETING

CPU BOARD SHEET 1

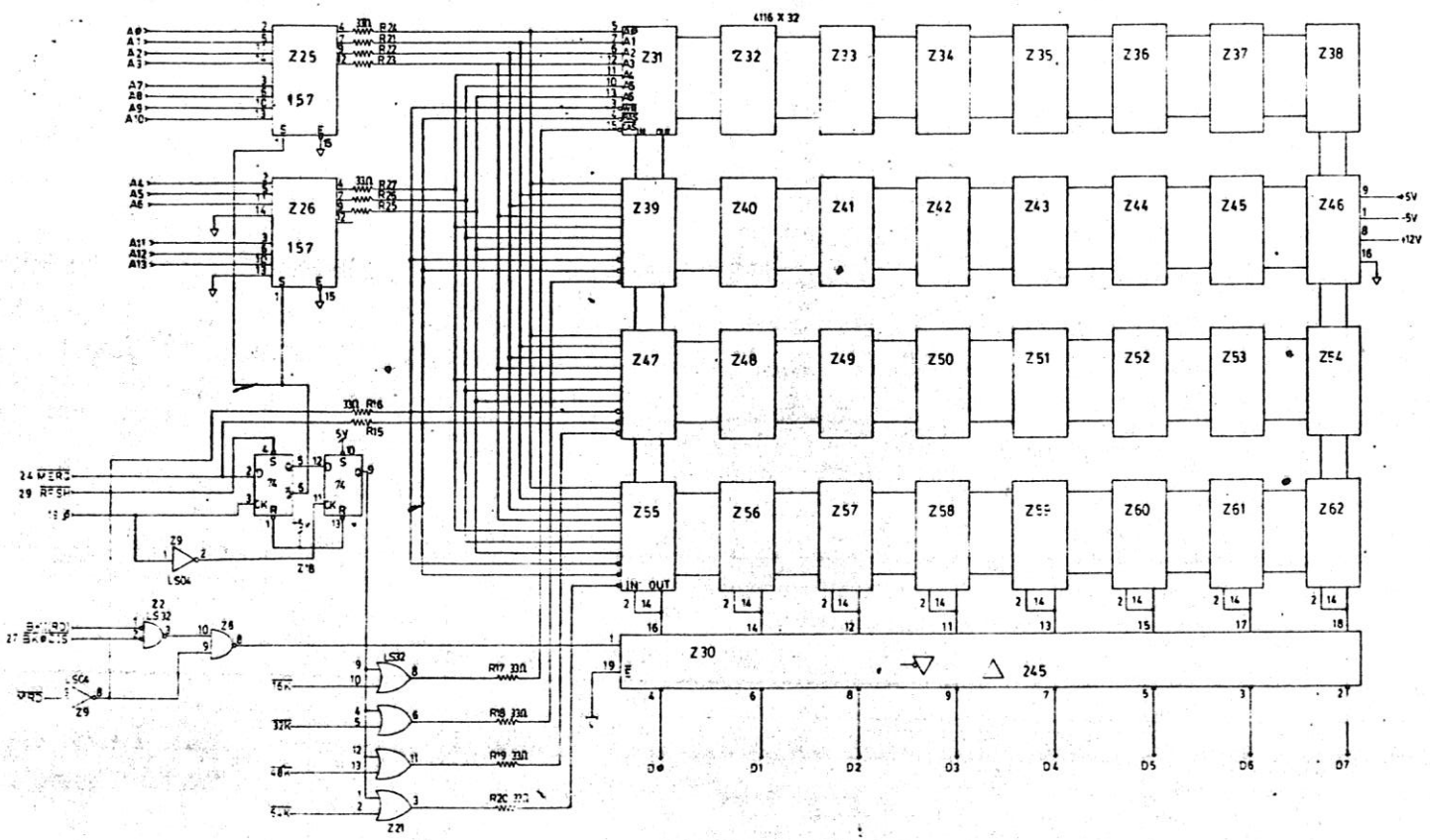


CPU BOARD SHEET 3



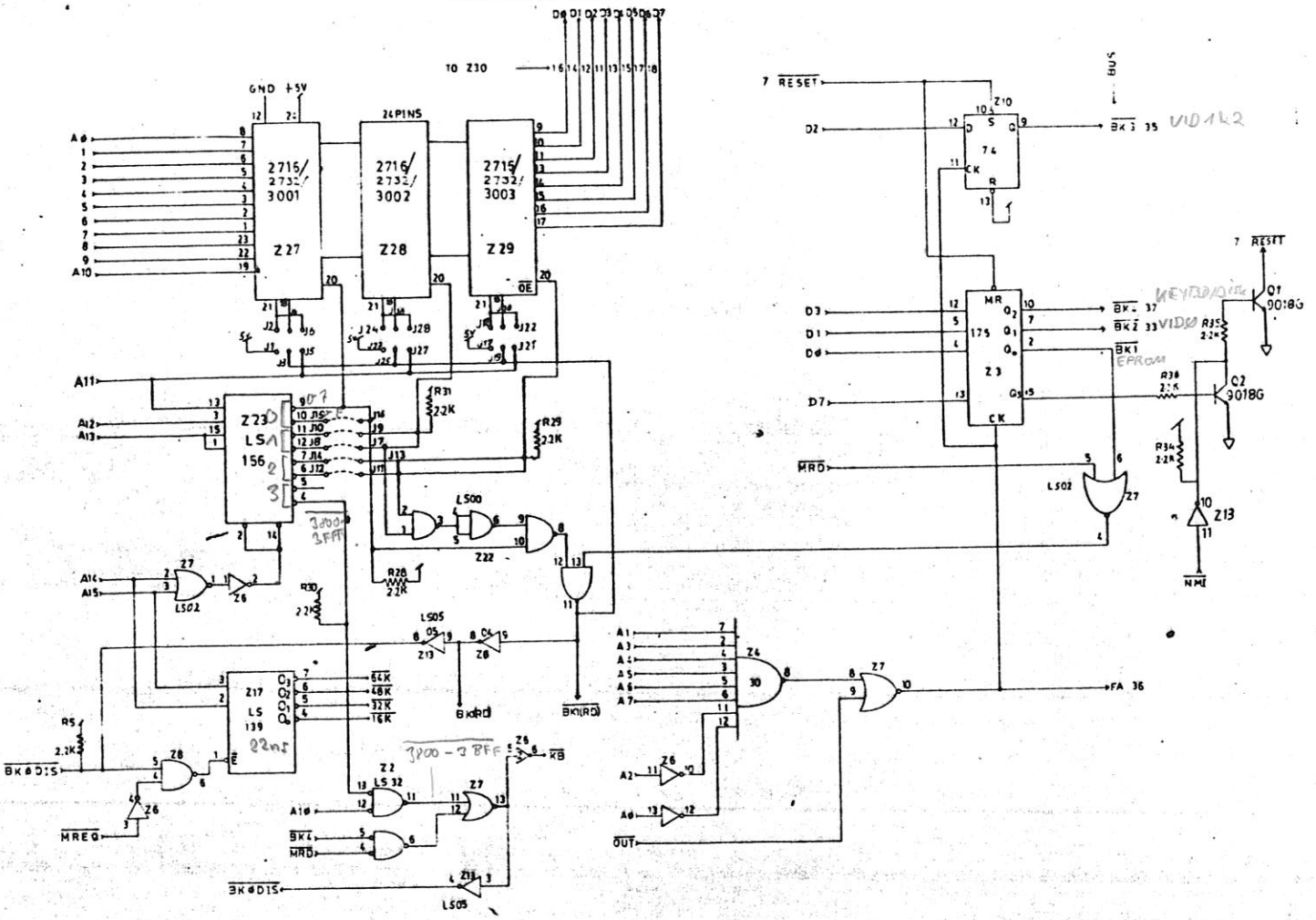
MARKETING

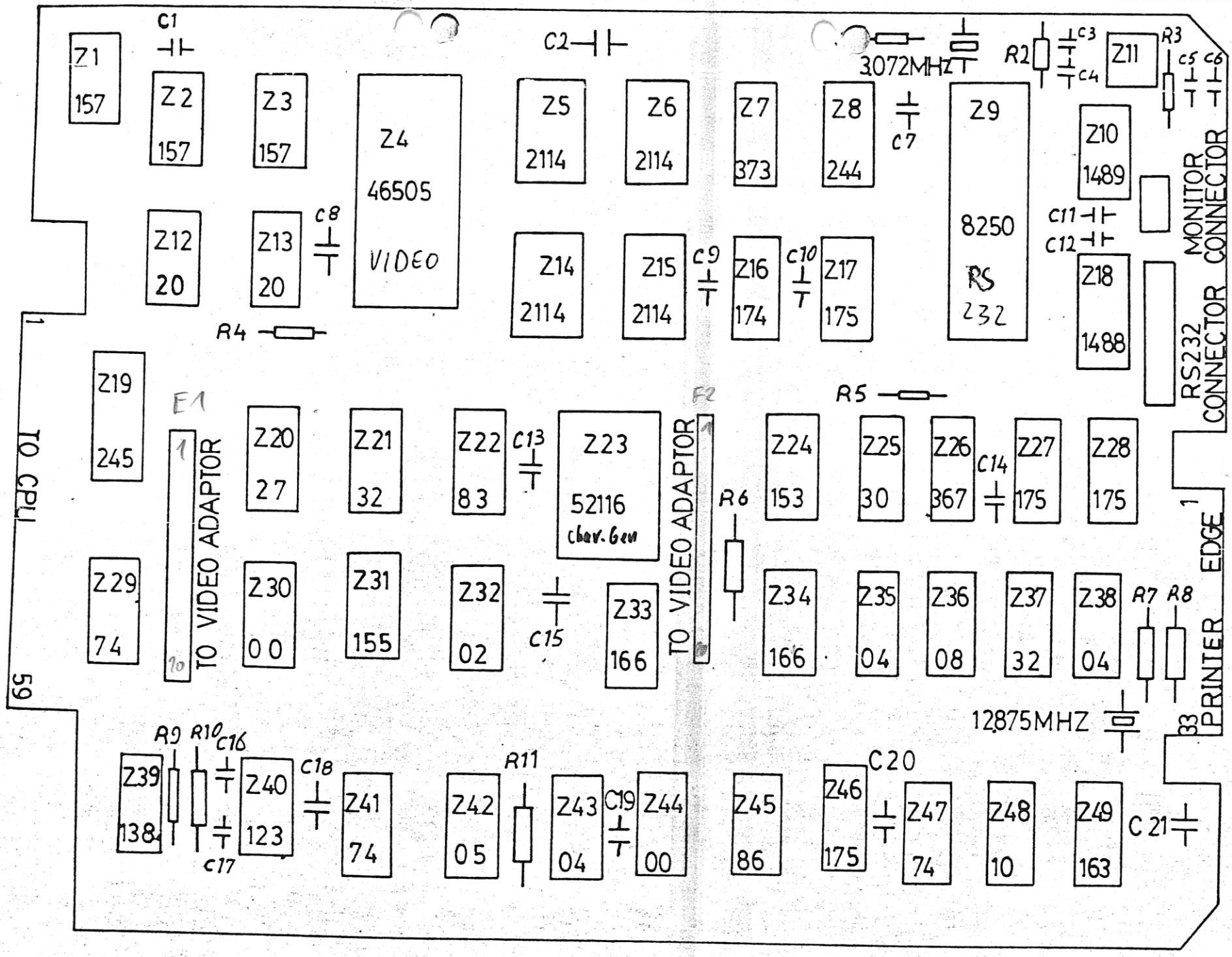
CPU BOARD SHEET 3



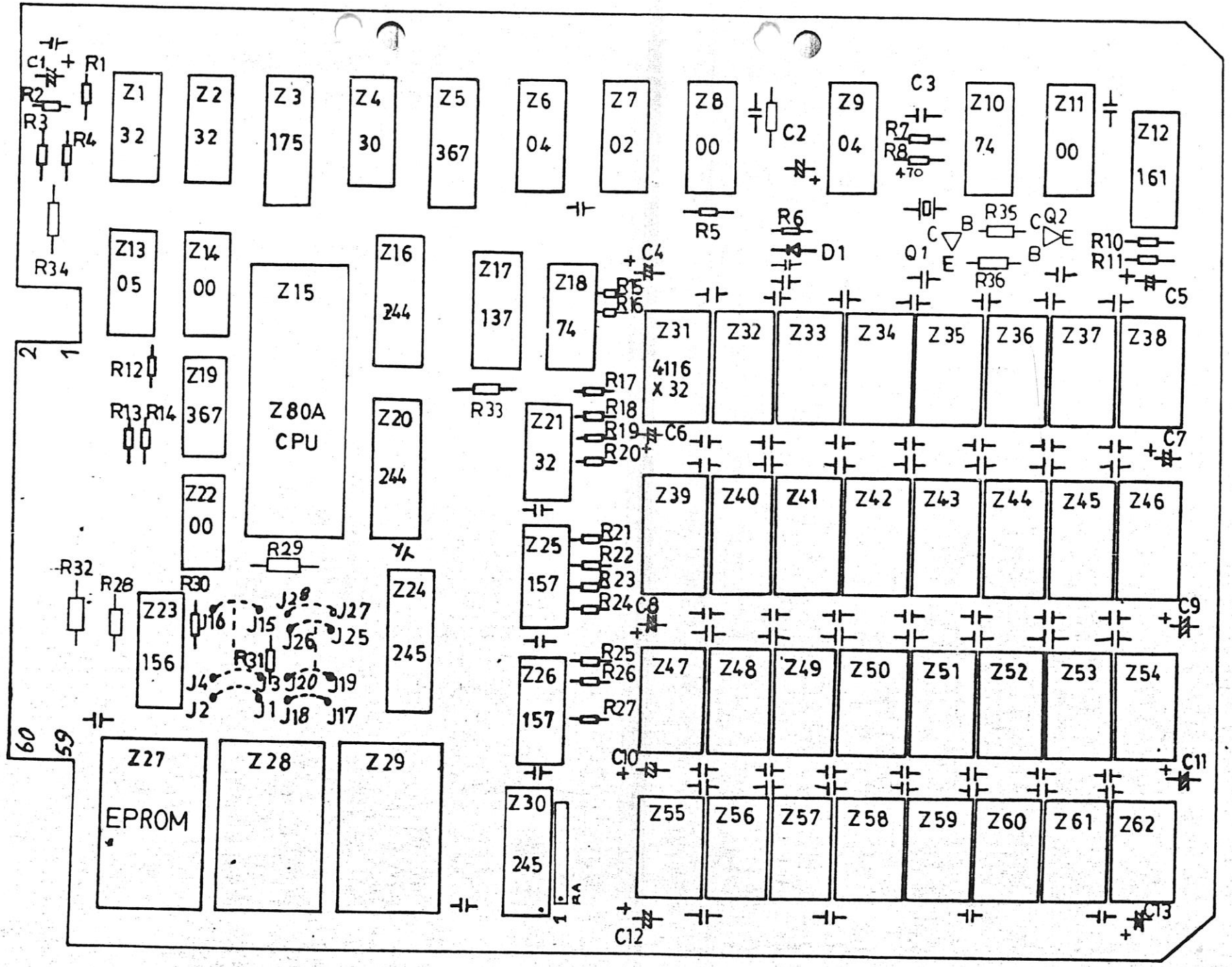
MARKETING

CPU BOARD SHEET 2



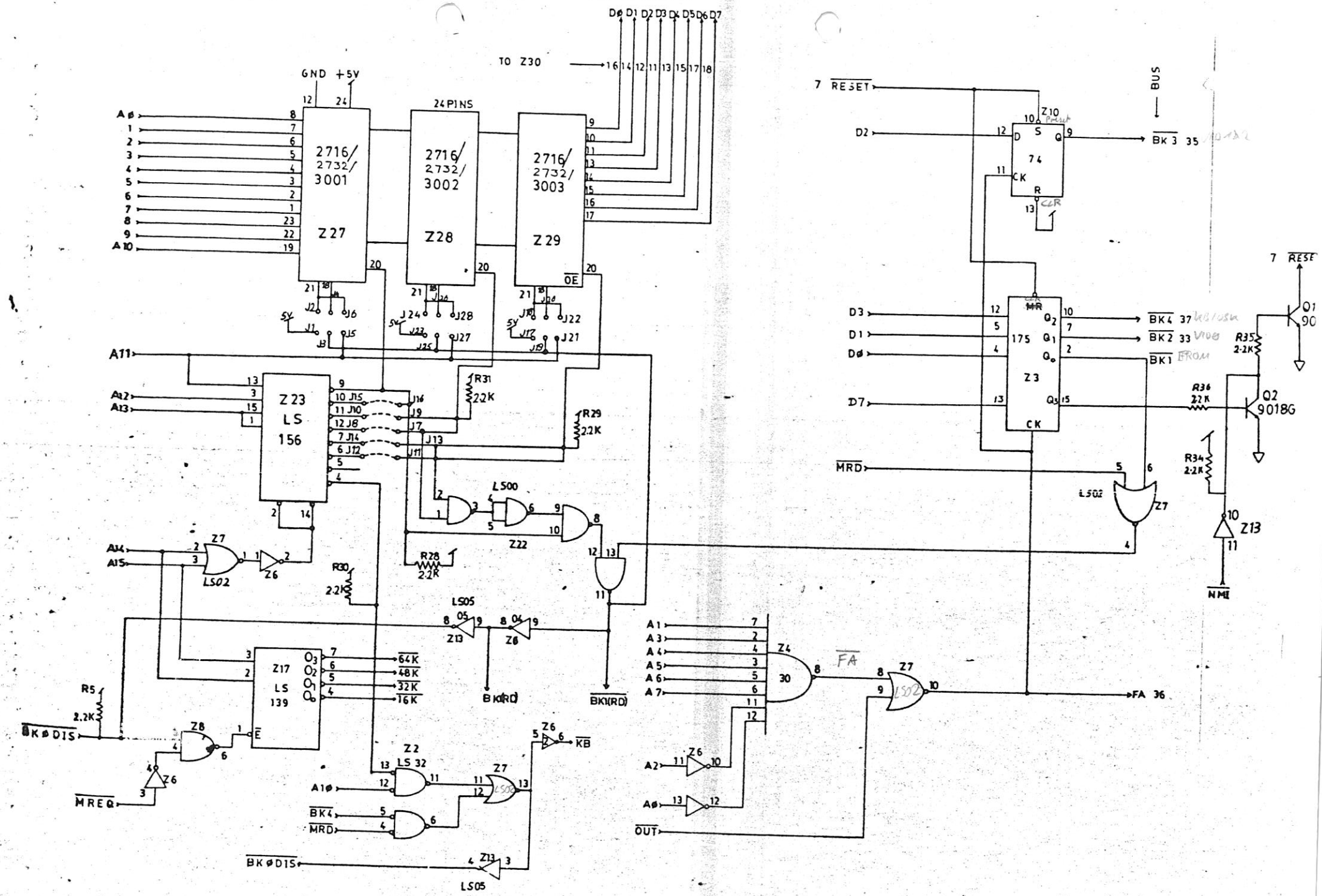


GENIE III INTERFACE 1

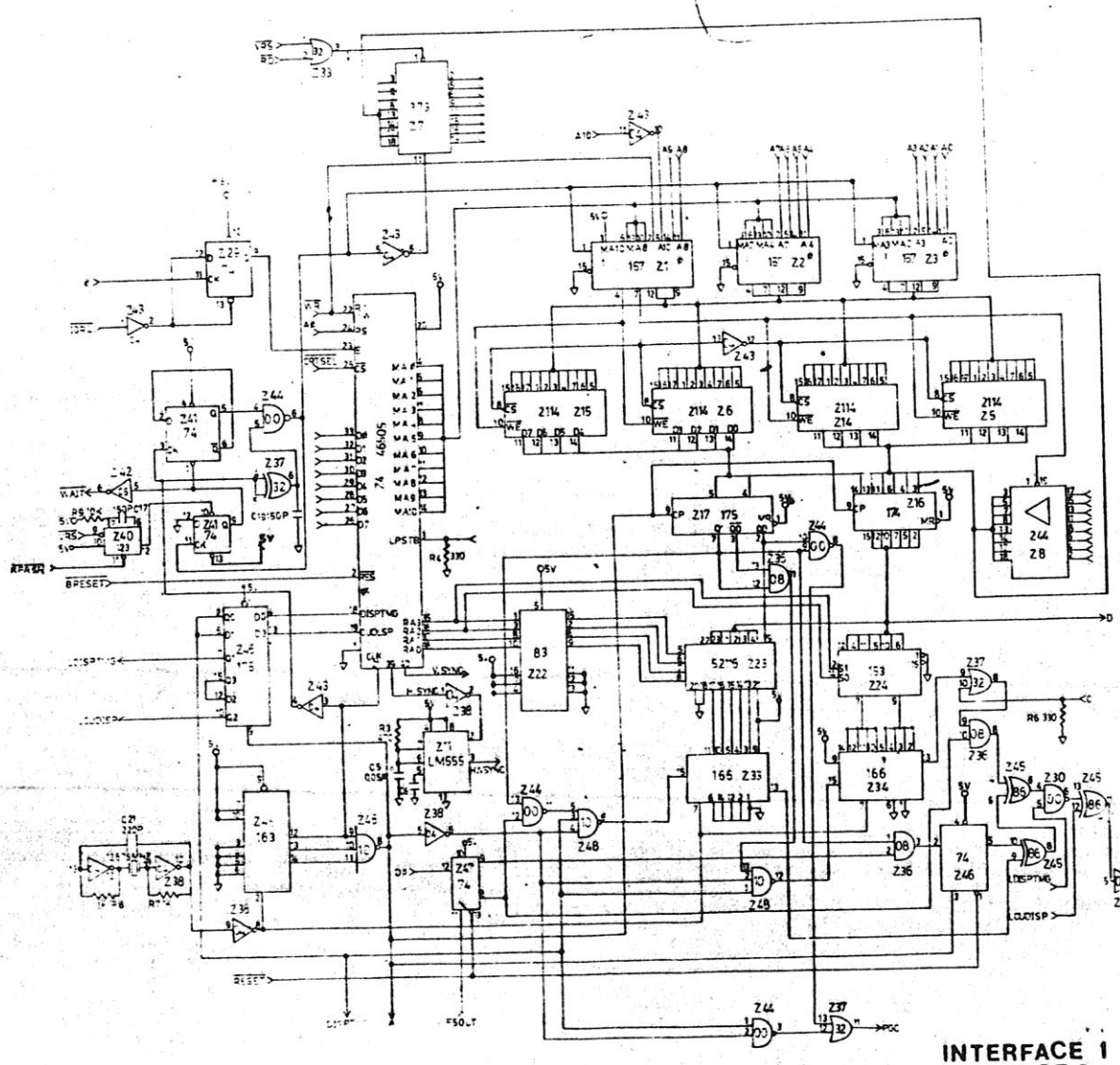


GENIE III CPU BOARD

CPU BOARD SHEET 2



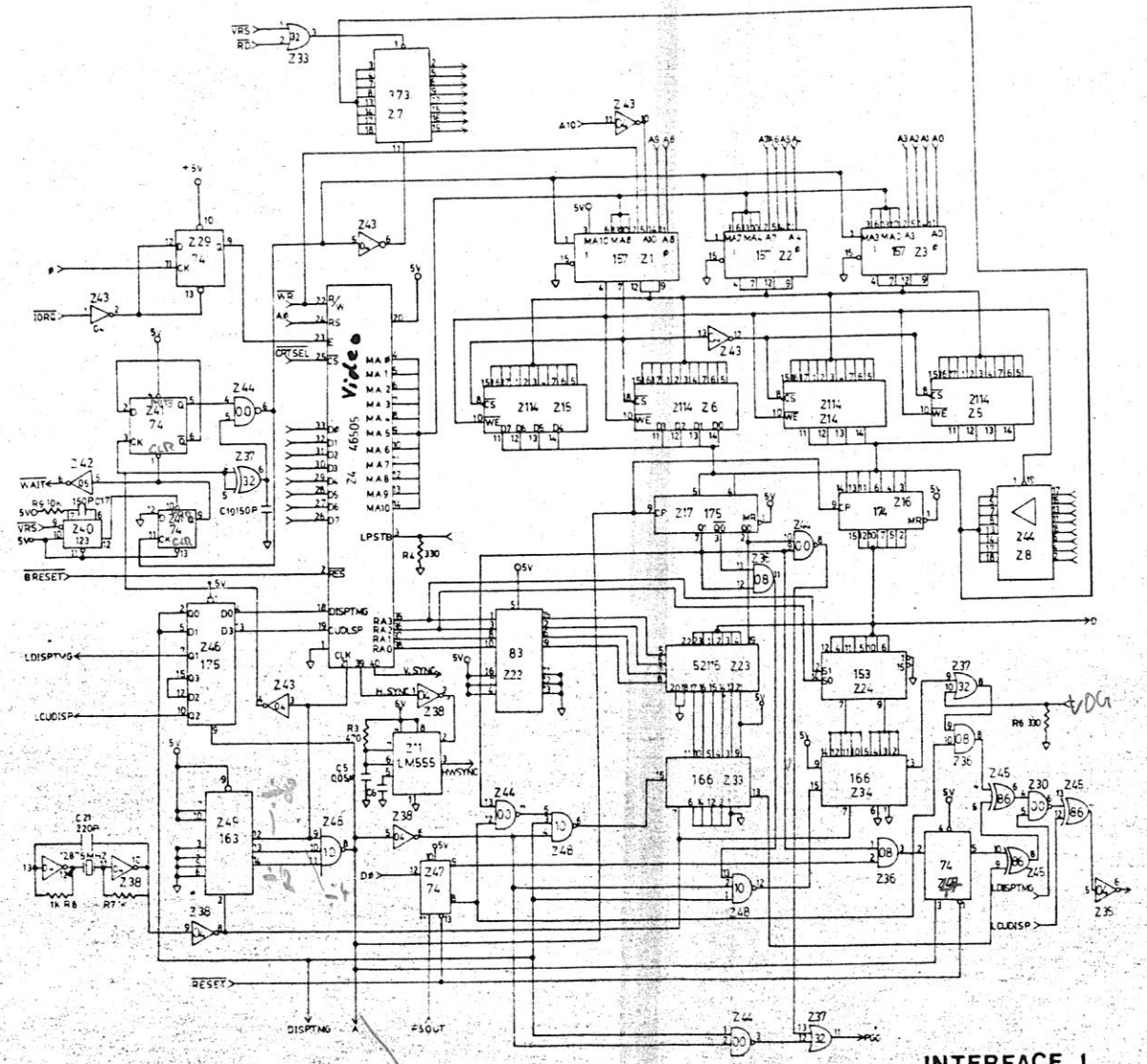
MARKETING



INTERFACE 1
PAGE 2 OF 2

CLK 46505

1,609375 MHz

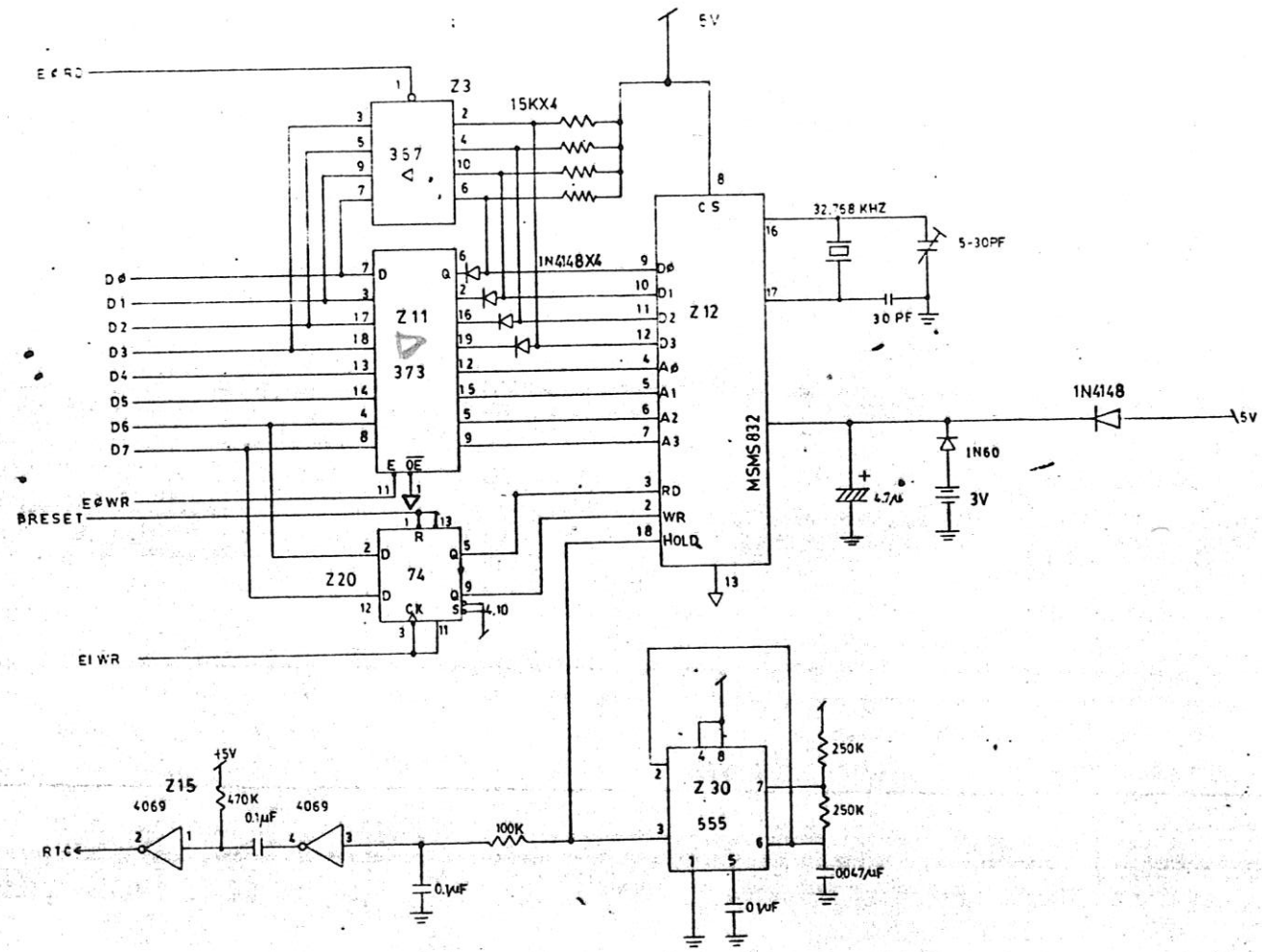


÷ 14

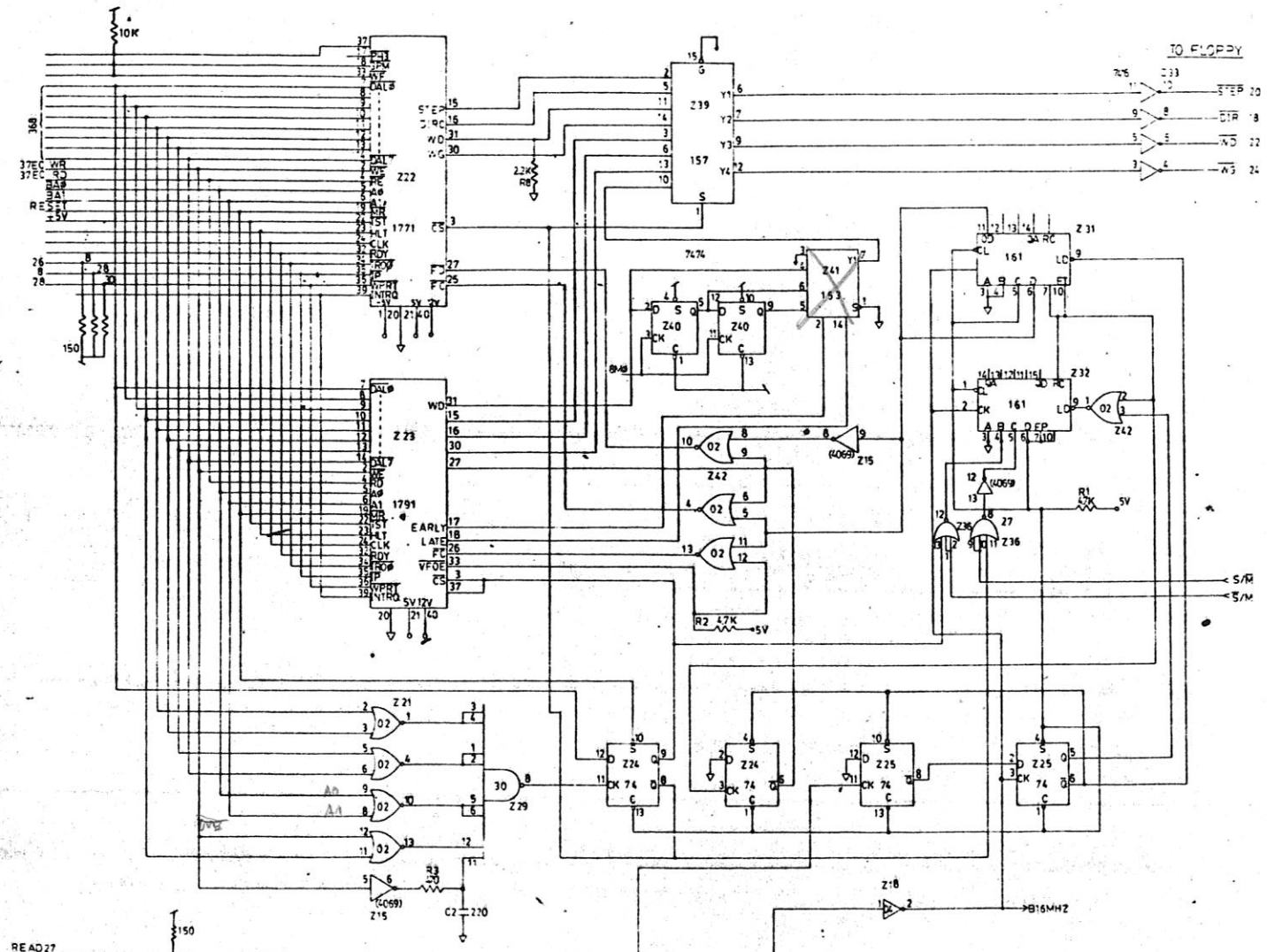
= 0,9196

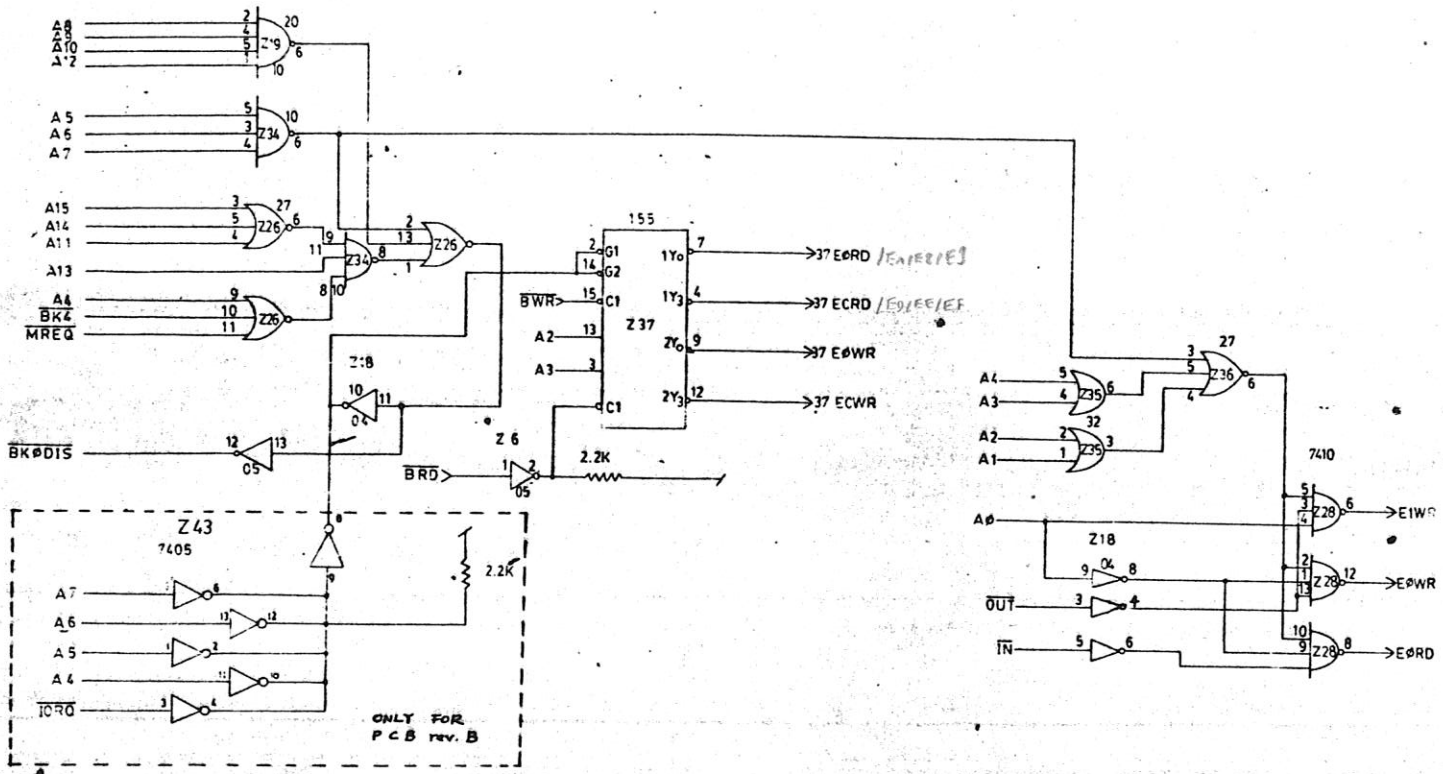
INTERFACE 1
PAGE 2 OF 2

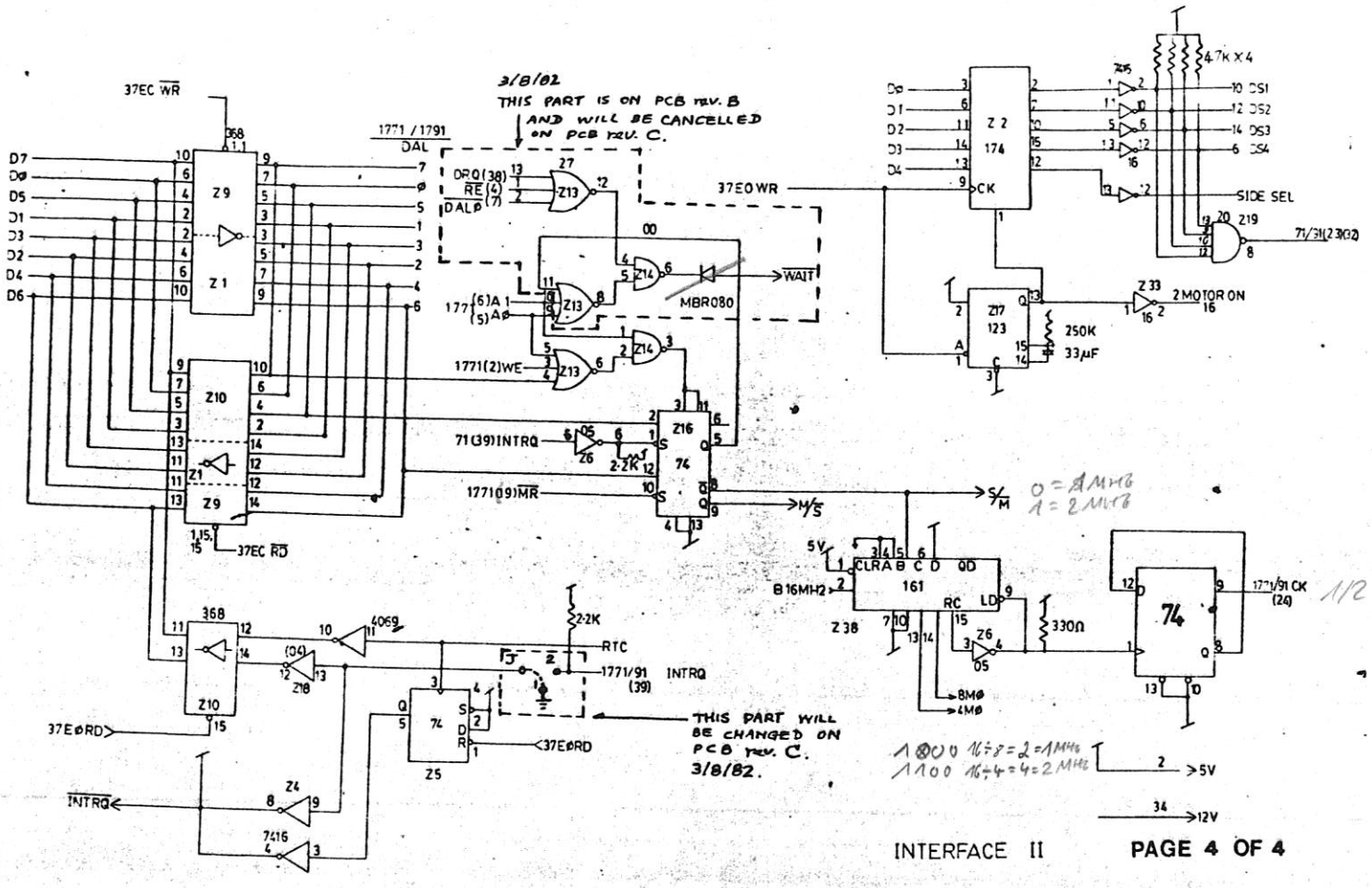
INTERFACE II



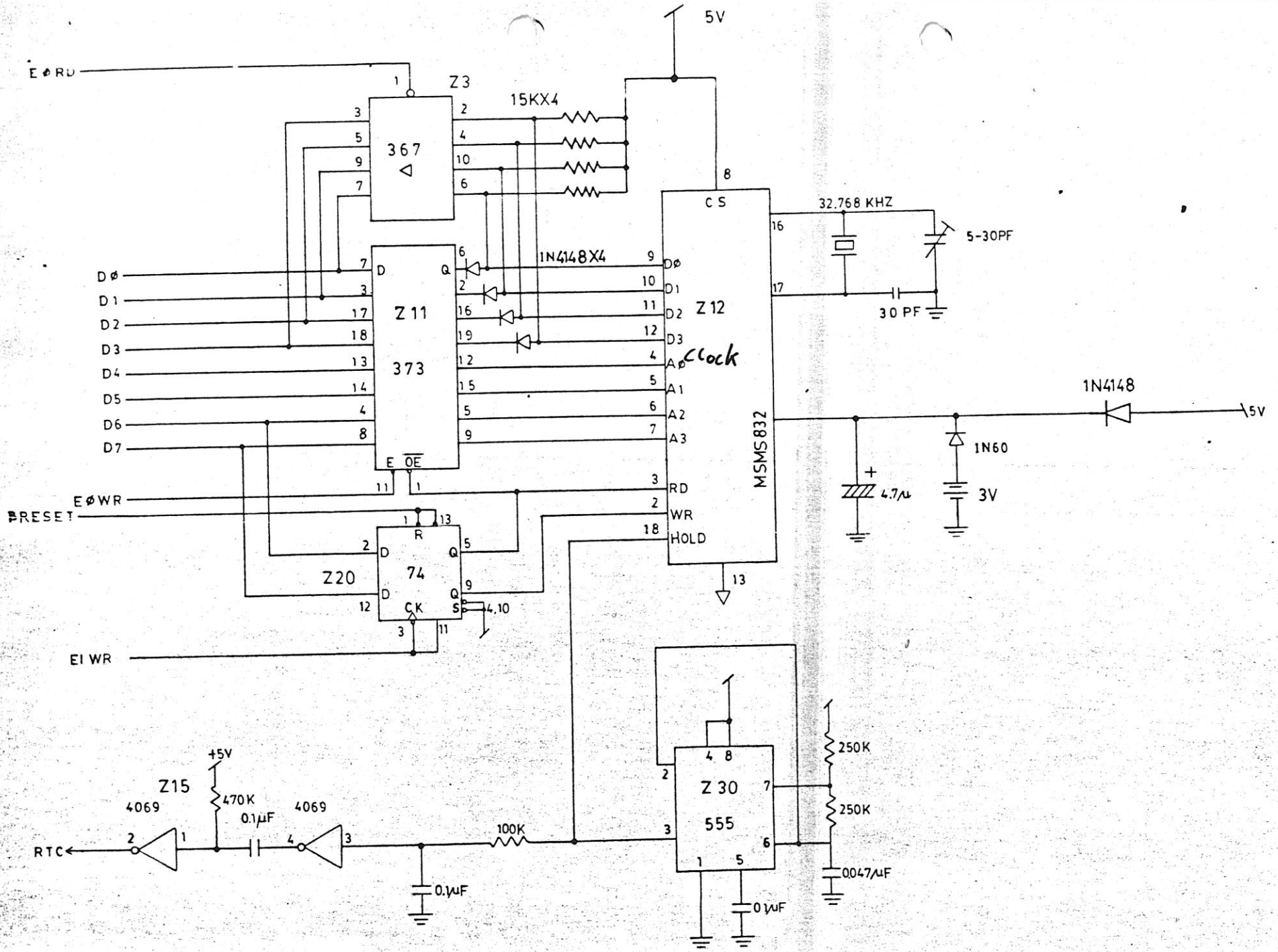
INTERFACE II

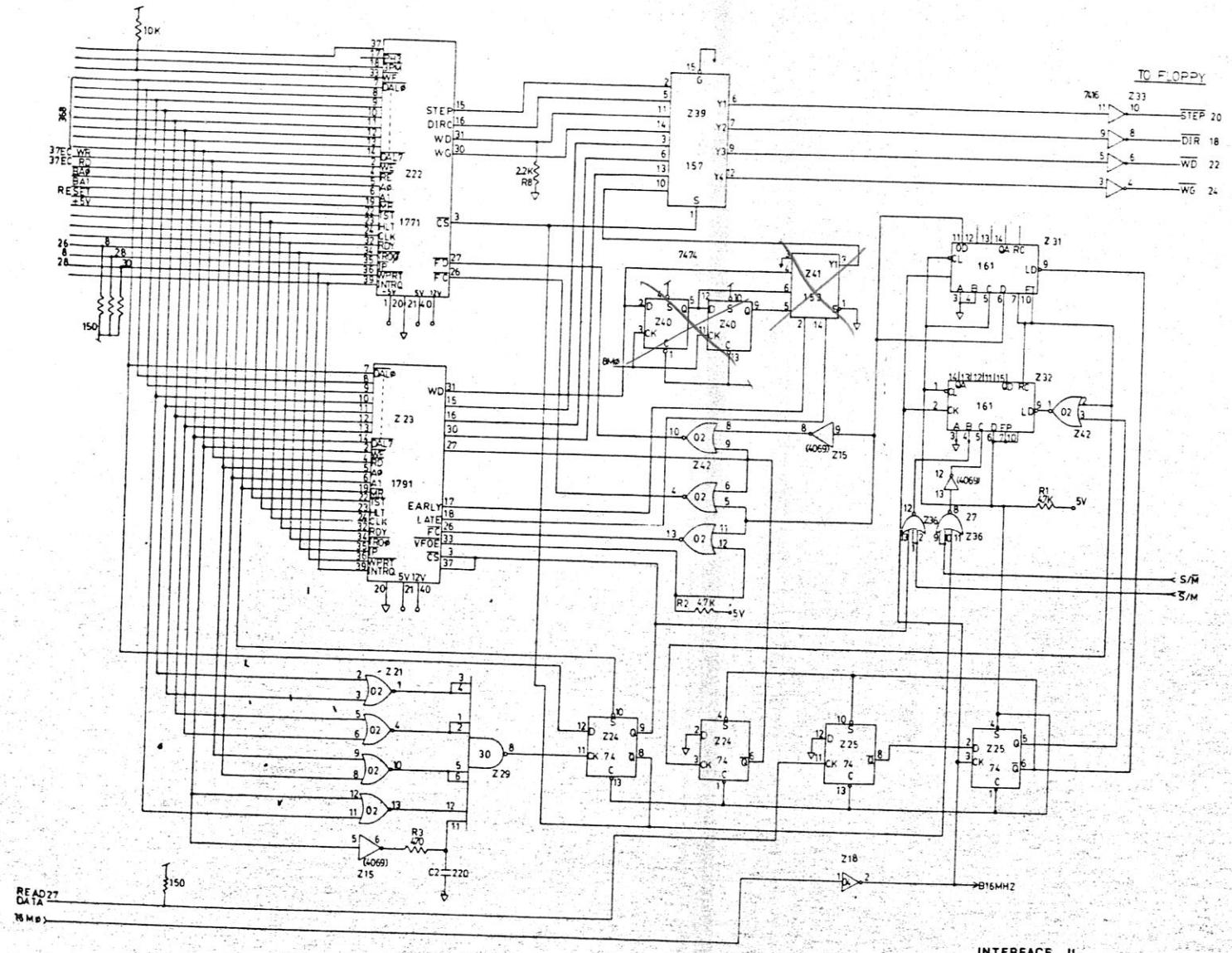

TO FLOPPY
STEP 20
DIR 18
WD 22
WG 24
S/M
S/M
READ DATA
16MHZ
INTERFACE II
PAGE 2 OF 4

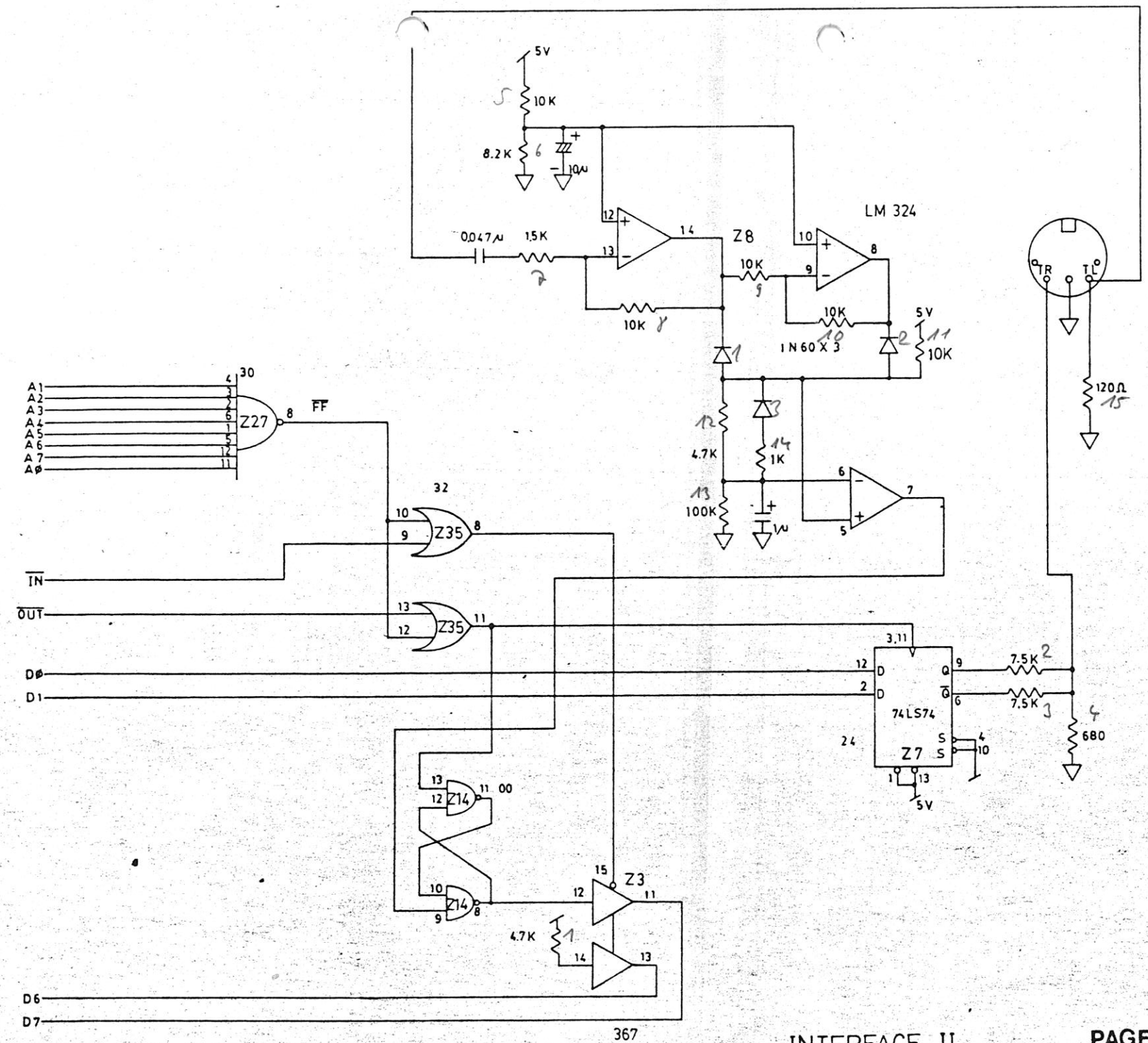

A8
A9
A10
A12
Z19
A5
A6
A7
Z34
A15
A14
A11
A13
Z26
A4
BK4
MREQ
Z26
Z34
Z25
Z18
BKØDIS
05
Z 6
BRD
05
2.2K
155
G1
G2
BWR
C1
A2
A3
C1
Z37
1Y0
1Y3
2Y0
2Y3
37 EØRD /E01EE1E1
37 ECRD /E01EE1EF
37 EØWR
37 ECWR
Z43
7405
A7
A6
A5
A4
IORQ
2.2K
ONLY FOR
PCB rev. B
THIS PART WILL BE DELETED ON PCB rev. C.
3/8/82.
A4
A3
Z35
A2
A1
Z35
Z36
7410
AØ
Z18
OUT
IN
Z28
Z28
Z28
E1WR
EØWR
EØRD

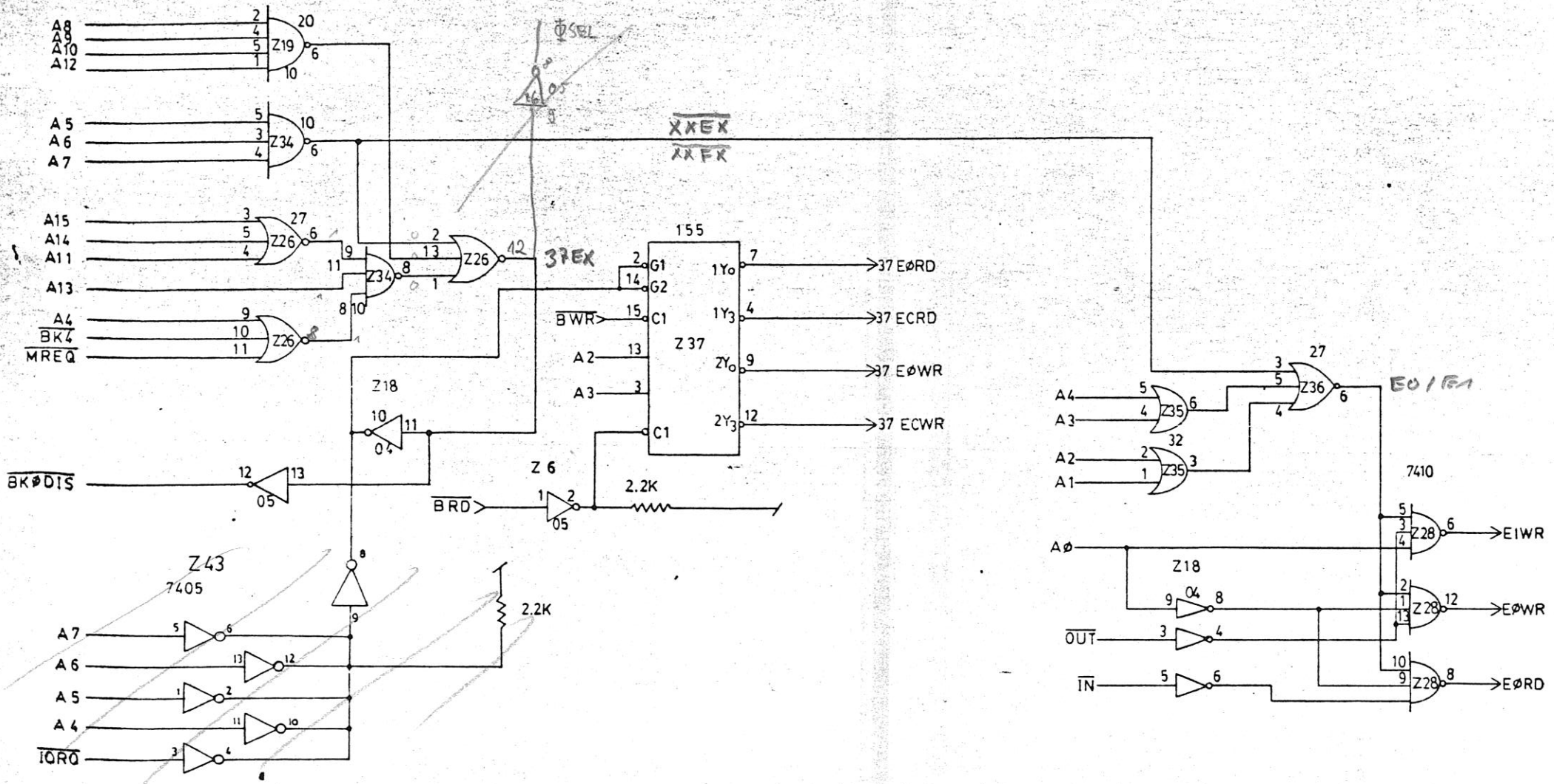


INTERFACE II

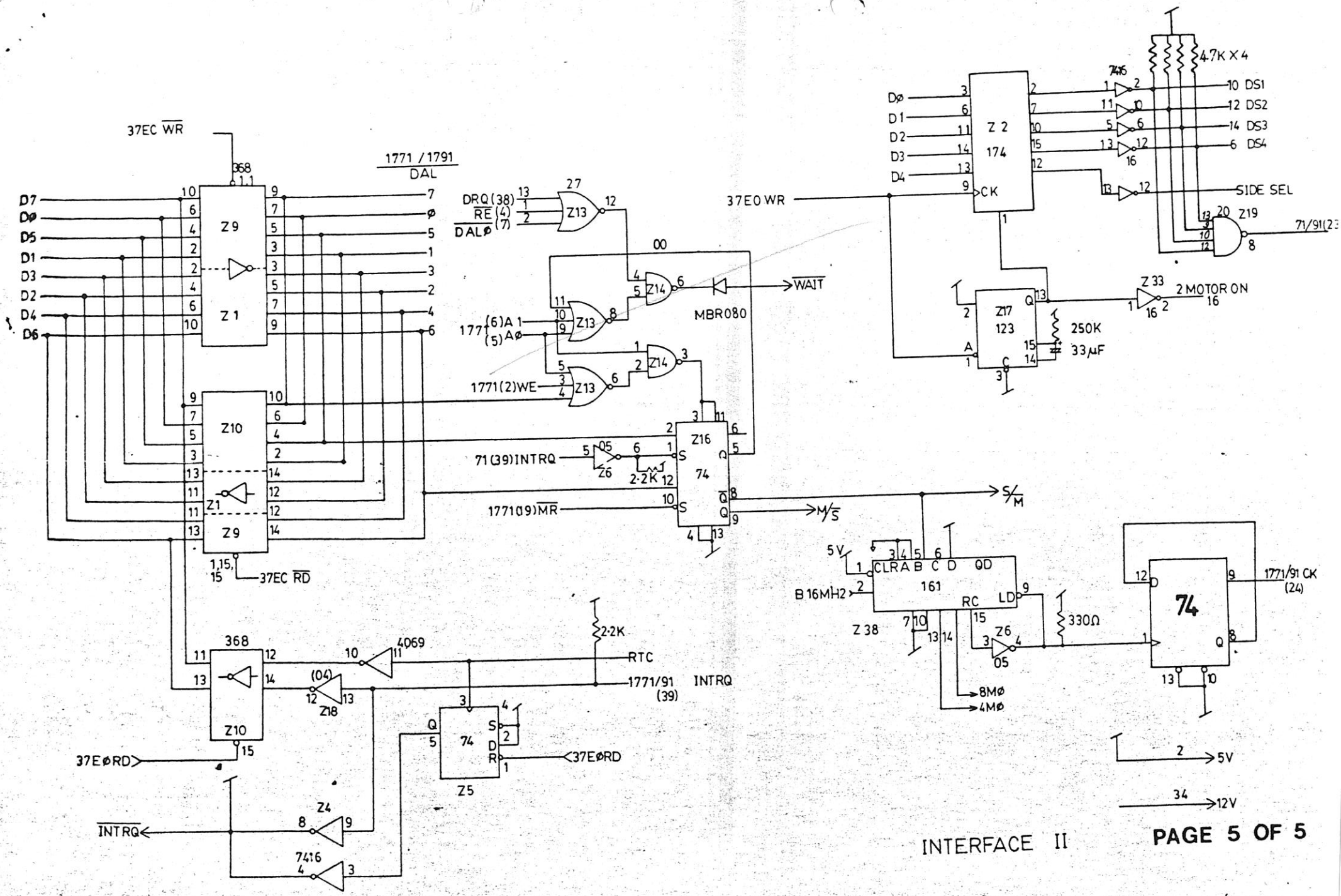

5V
EØRD
Z3
367
15KX4
1N4148X4
DØ
D1
D2
D3
D4
D5
D6
D7
Z11
373
Z12
MSM5832
CS
32.768 KHZ
5-30PF
30 PF
Clock
1N4148
5V
1N60
3V
4.7µ
EØWR
PRESET
Z20
74
4.10
EI WR
Z15
4069
+5V
470K
0.1µF
RTC
100K
0.1µF
Z30
555
250K
250K
0.047µF
0.1µF


TO FLOPPY
STEP 20
DIR 18
WD 22
WG 24
Z22
1771
Z23
1791
Z39
157
Z41
153
Z40
7474
Z31
161
Z32
Z42
Z36
Z21
Z29
Z24
Z25
Z18
Z15
10K
2.2K R8
150
R1 47K
R2 47K
R3 470
C2 220
5V
S/M
S/M
READ DATA
16 MHz
B16MHZ
INTERFACE II
PAGE 2 OF 5

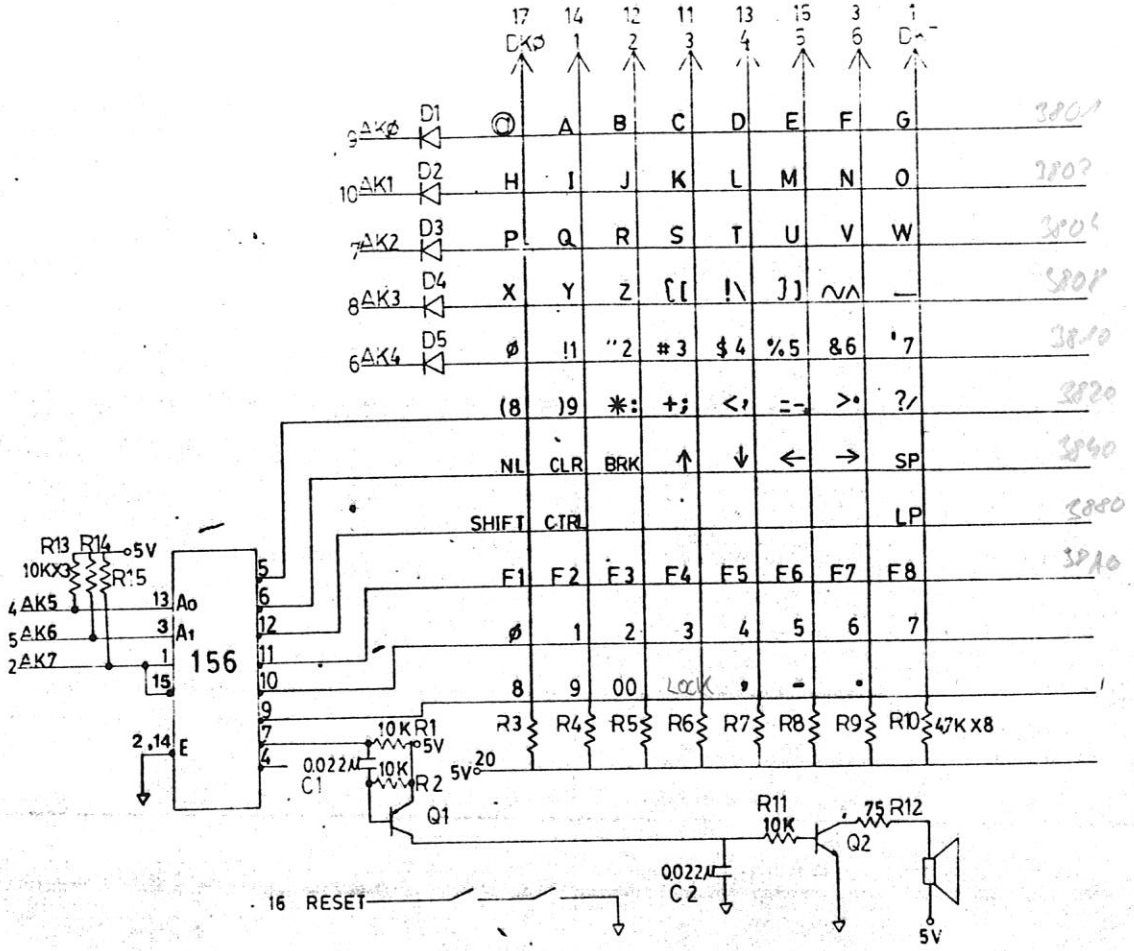

5V
10K
8.2K
10µ
0,047µ
1,5K
Z8
LM 324
10K
10K
10K
1N60X3
5V
10K
TR
TL
120Ω
4.7K
1K
100K
1µ
A1
A2
A3
A4
A5
A6
A7
Aø
Z27
FF
Z35
Z35
IN
OUT
Dø
D1
74LS74
Z7
7.5K
7.5K
680
Z14
Z14
00
Z3
4.7K
D6
D7
367
INTERFACE II
PAGE 3 OF 5



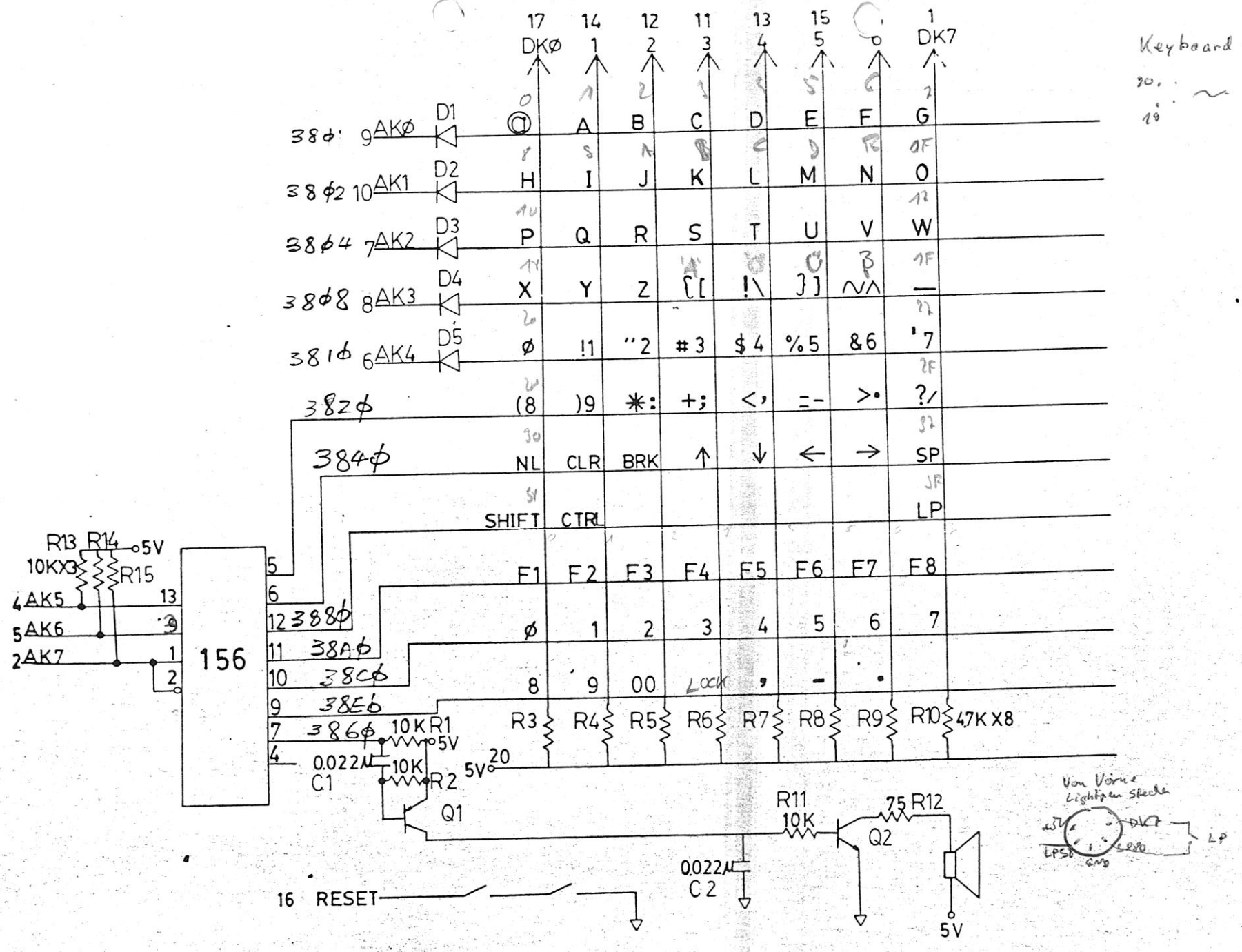
INTERFACE II



INTERFACE II

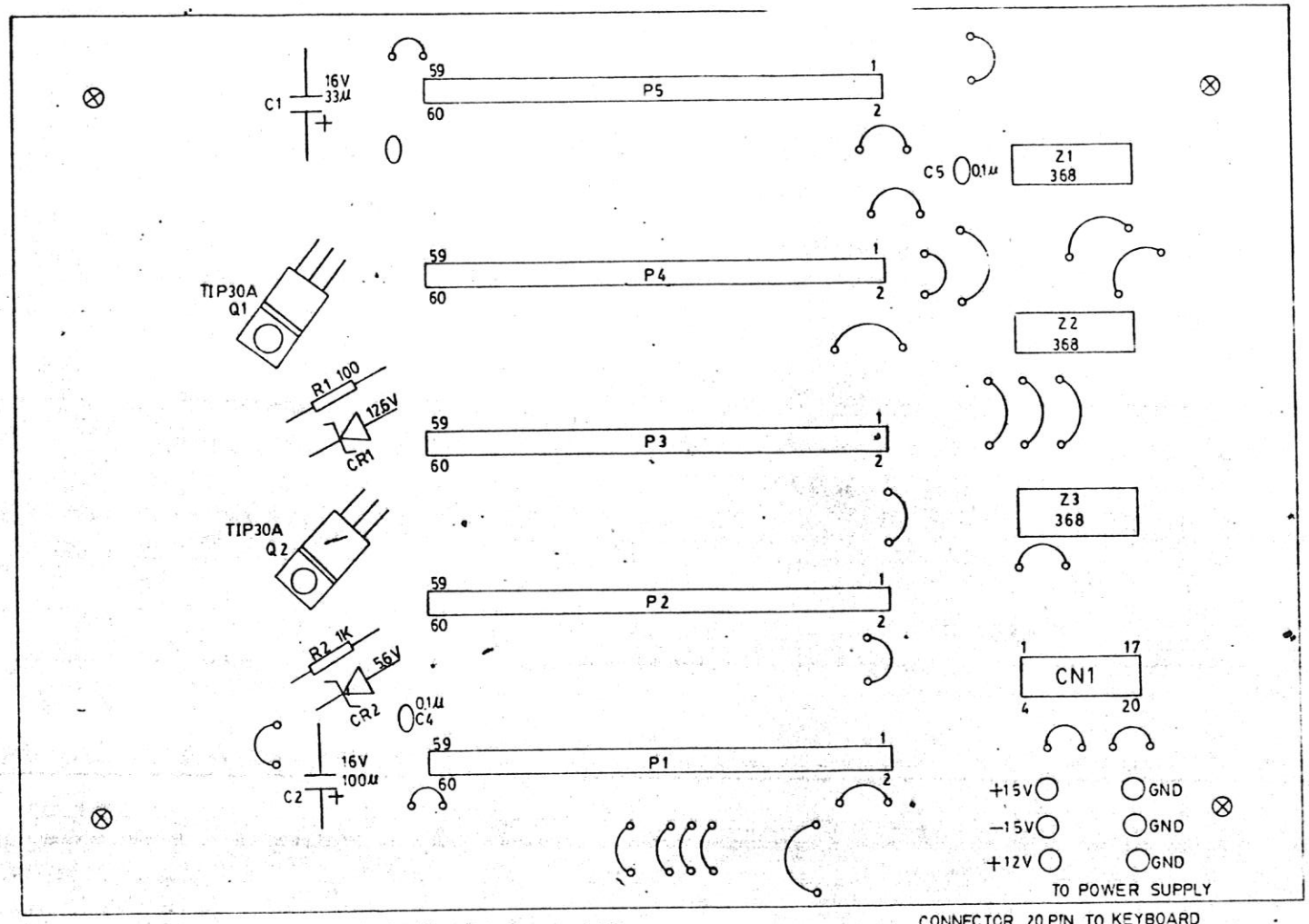


GENIE II KEYBOARD

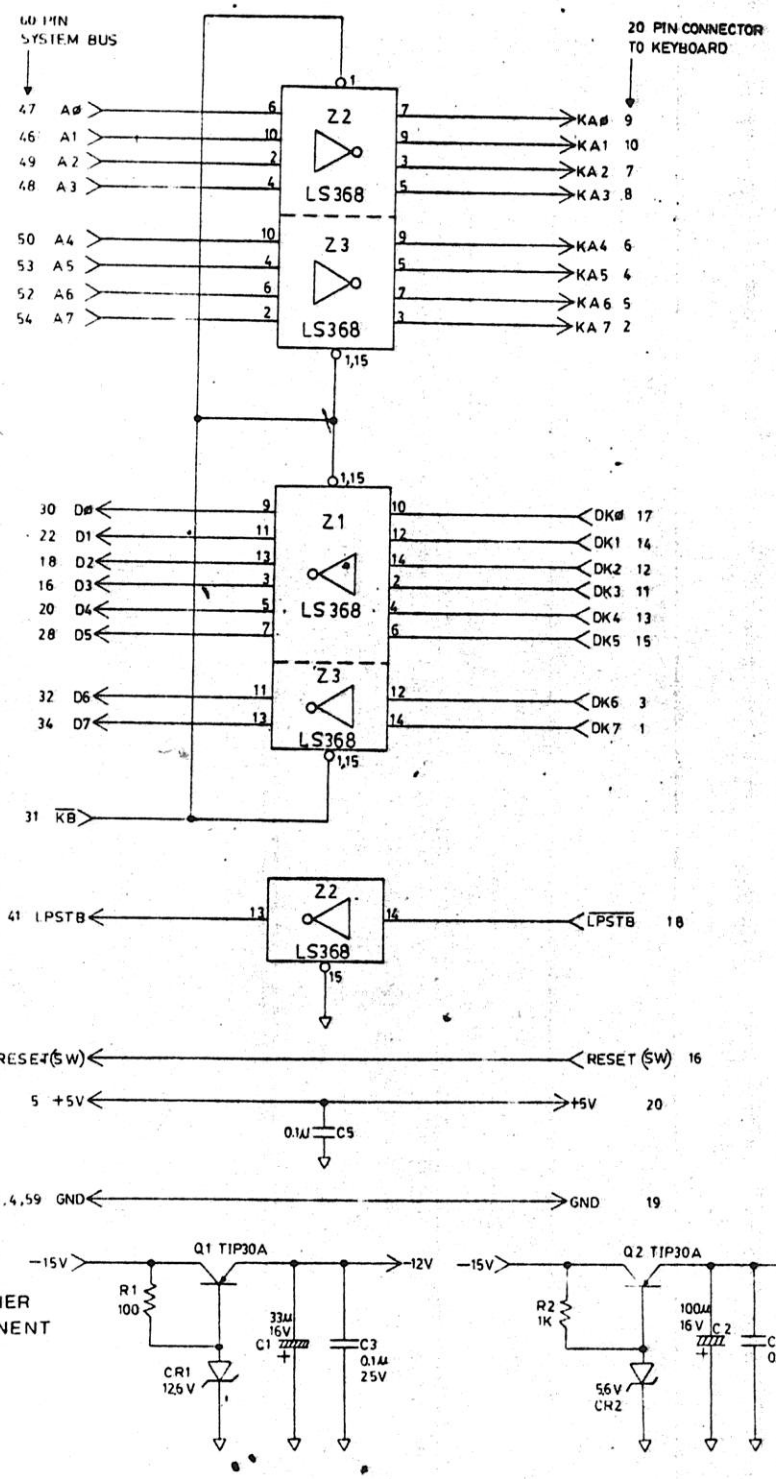


Keyboard Stecker Lötseite.

MARKETING
3 AUG 1982



GENIE III MOTHER BOARD
COMPONENT LAYOUT



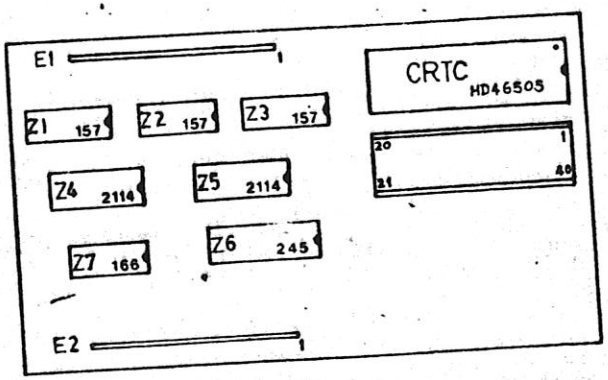
GENIE III MOTHER BOARD COMPONENT LAYOUT

PAGE 2 OF 2

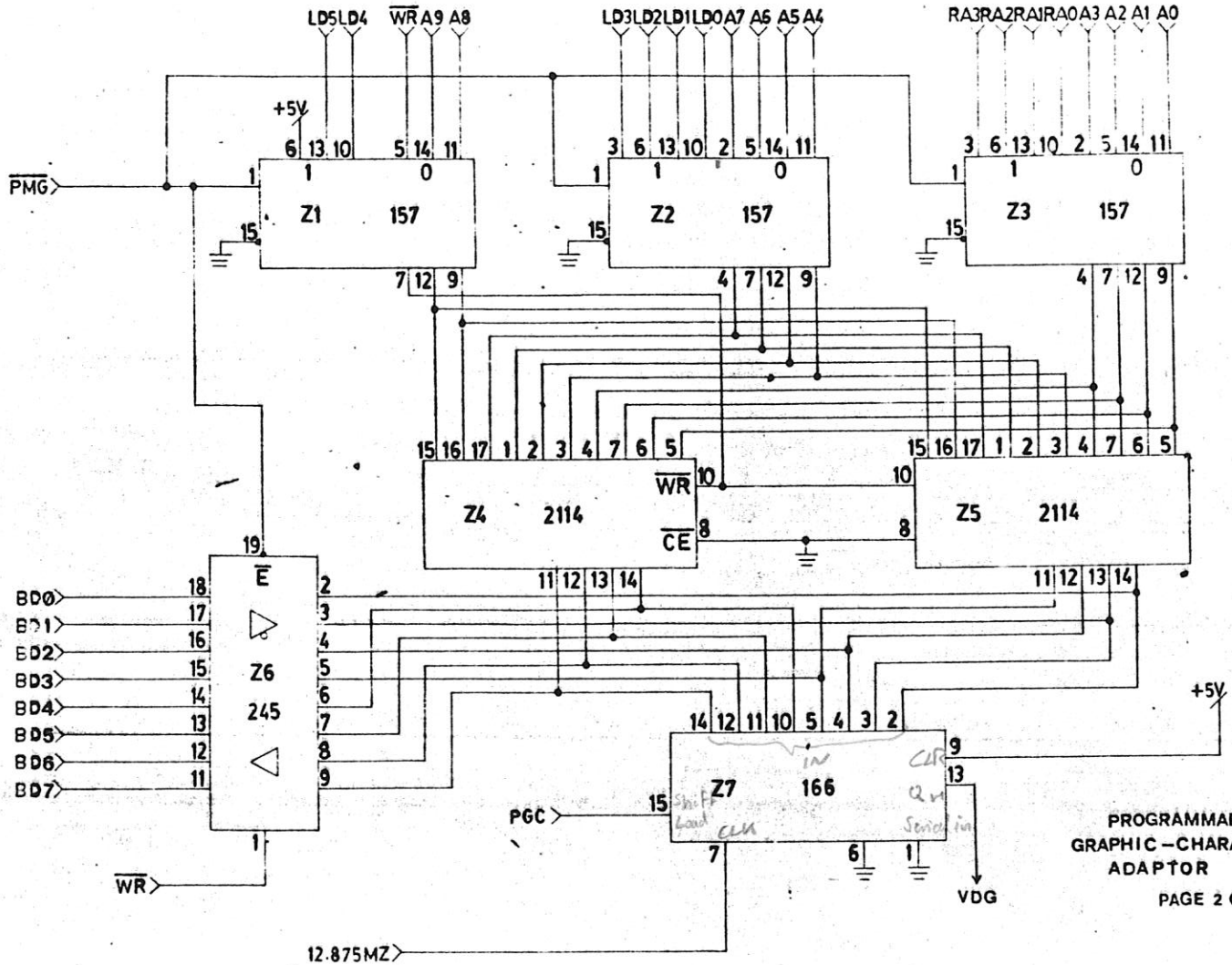
MARKETING

MARKETING

- 3 AUG 1982



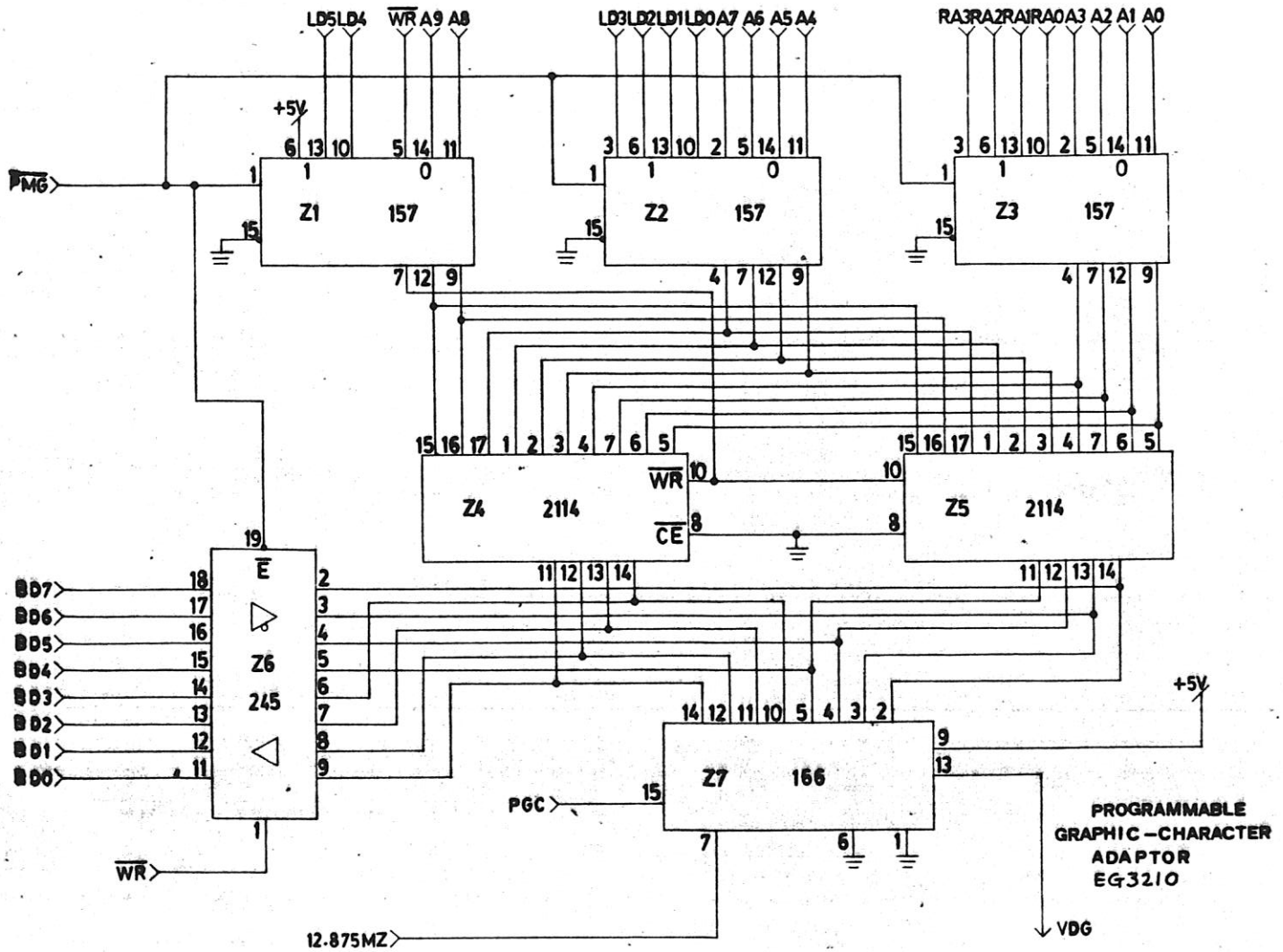
PROGRAMMABLE
GRAPHIC ADAPTOR



157 Datenselector

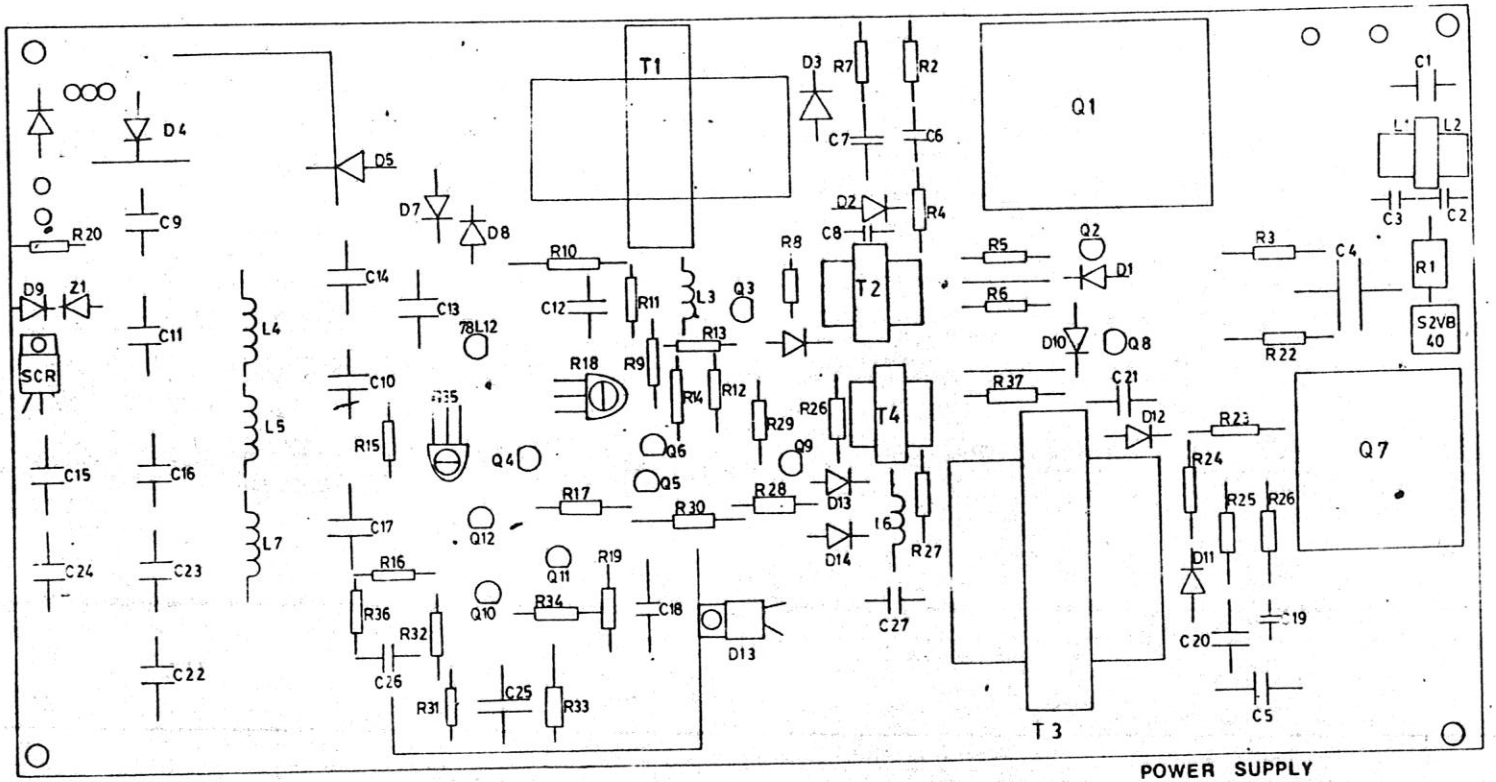
2114 1K x 4 RAM

166 8 Bit Schieberegister


LD5 LD4 WR A9 A8
LD3 LD2 LD1 LD0 A7 A6 A5 A4
RA3 RA2 RA1 RA0 A3 A2 A1 A0
+5V
PMG
Z1 157
Z2 157
Z3 157
Z4 2114
Z5 2114
Z6 245
Z7 166
WR
CE
E
BD7
BD6
BD5
BD4
BD3
BD2
BD1
BD0
PGC
12.875MZ
+5V
VDG
PROGRAMMABLE
GRAPHIC-CHARACTER
ADAPTOR
EG3210

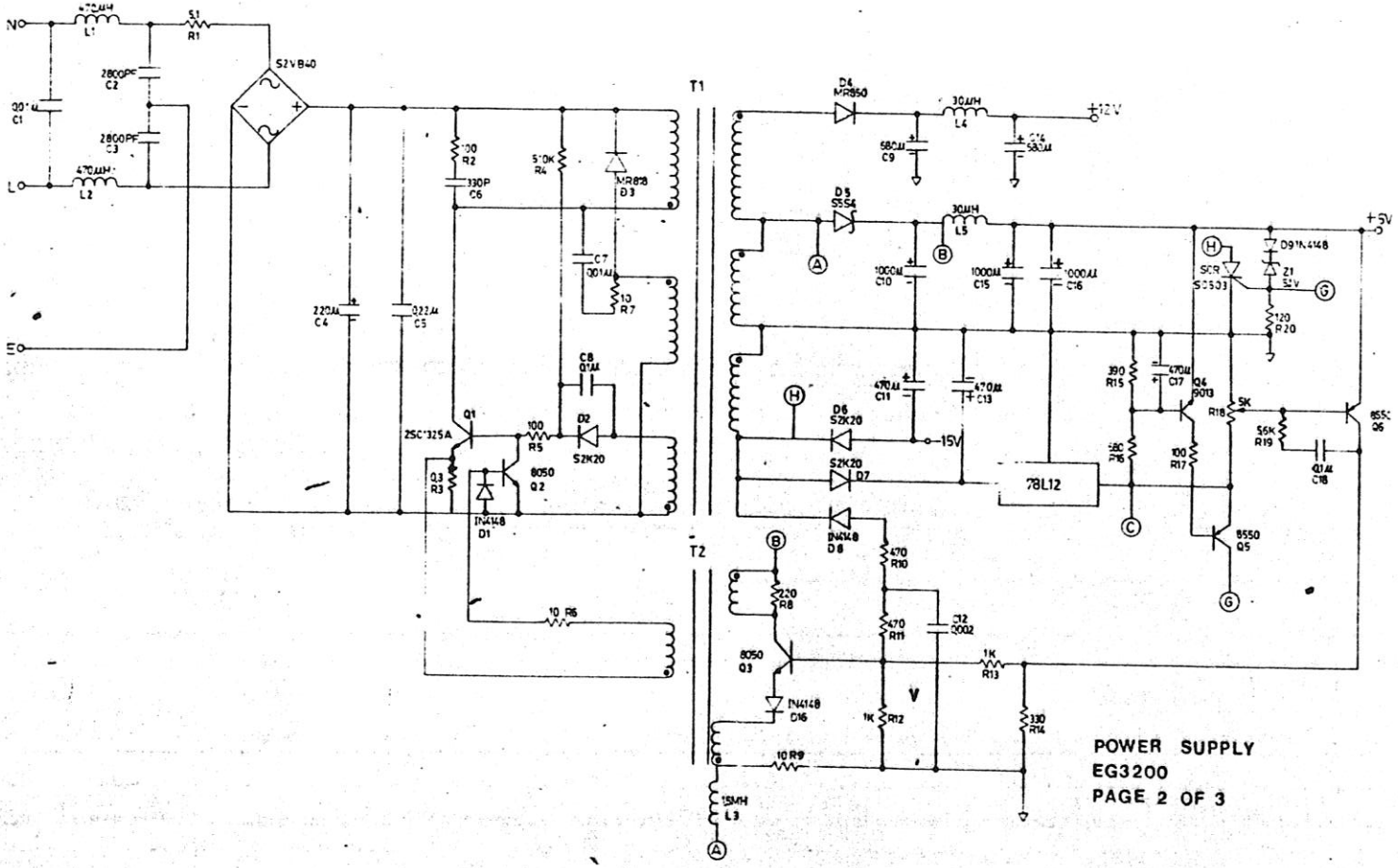
MARKETING

- 3 AUG 1982

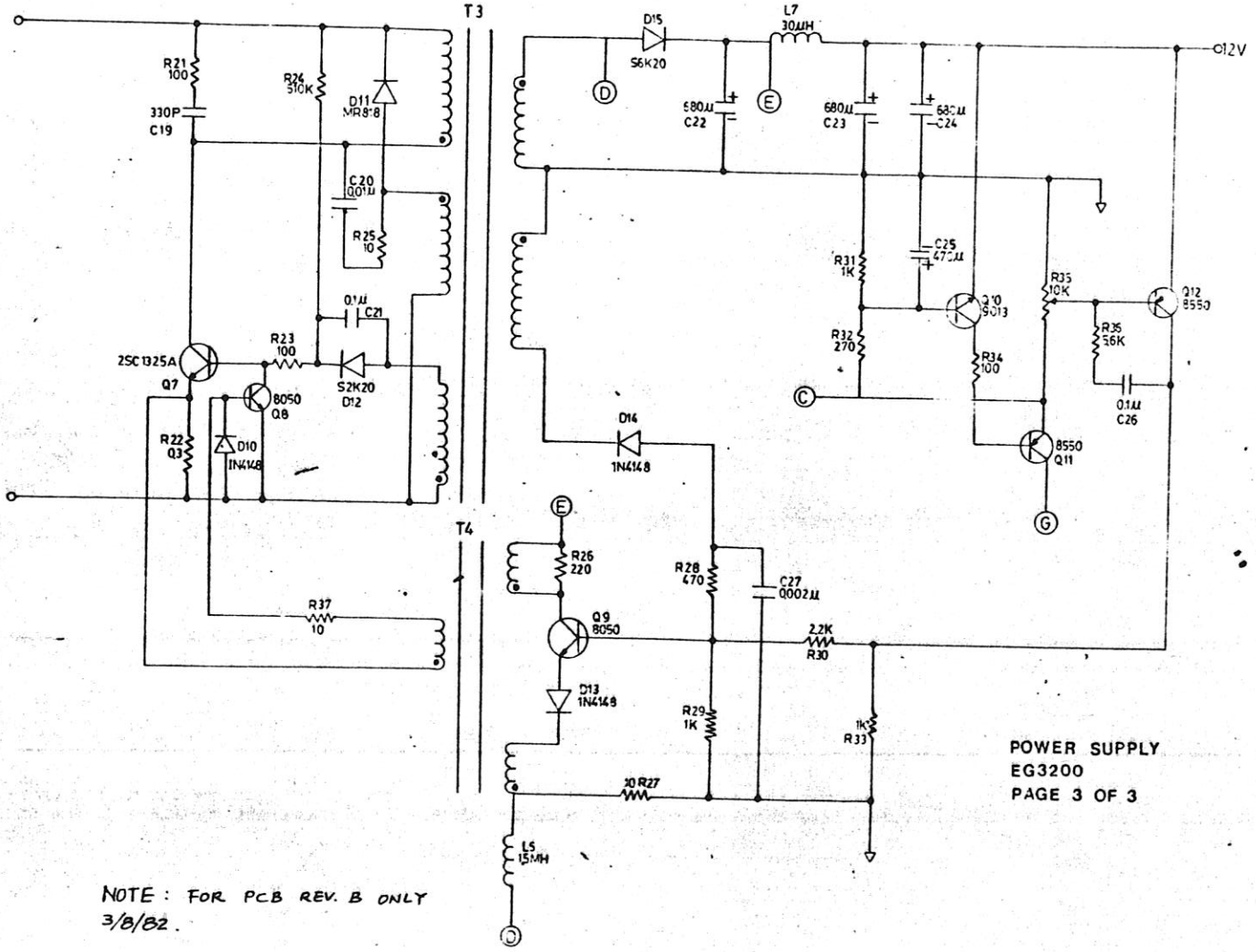


NOTE: FOR PCB REV. B ONLY.
3/8/82.

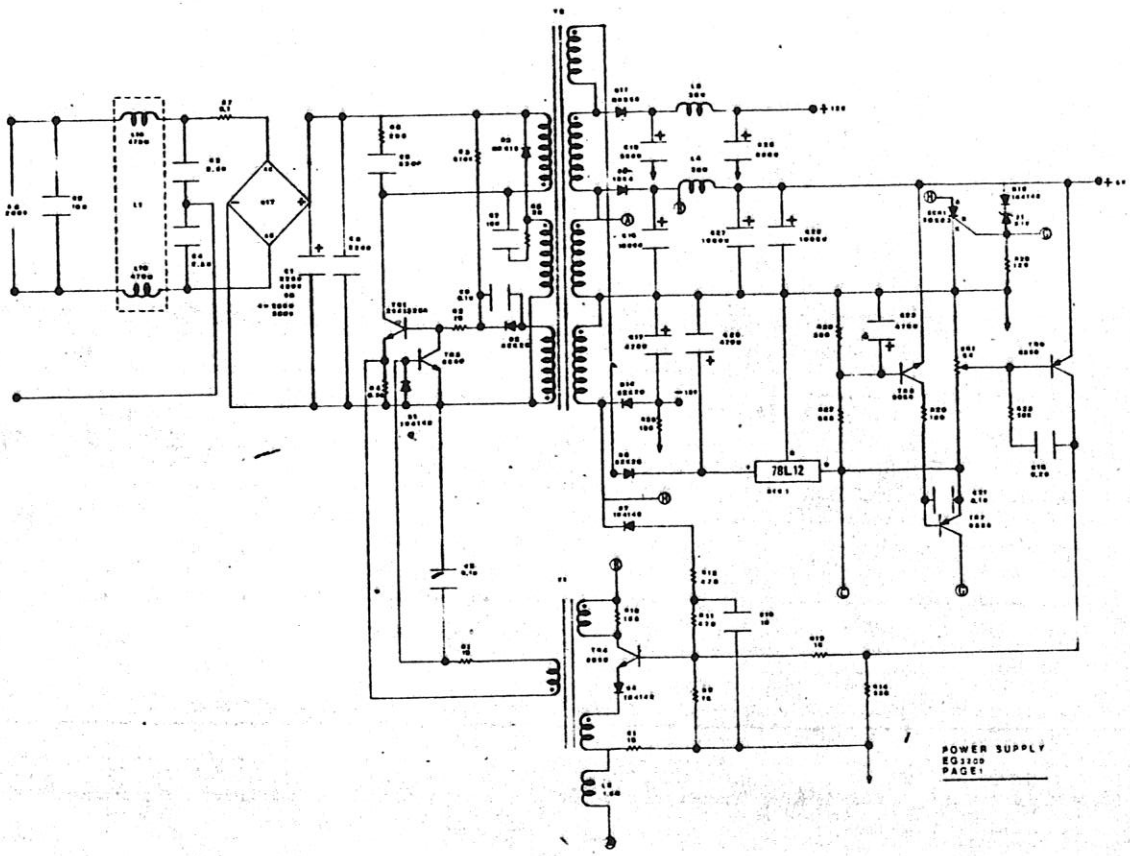
POWER SUPPLY
COMPONENT LAYOUT
EG3200
PAGE 1 OF 3



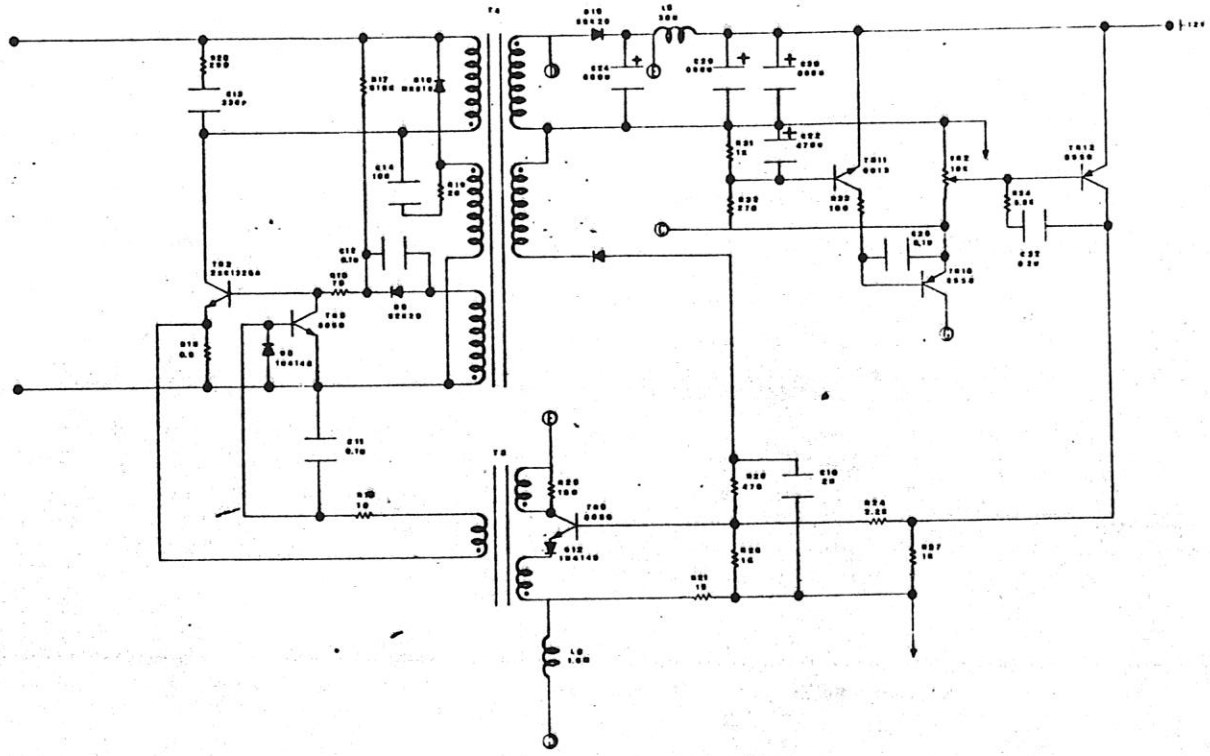
NOTE : FOR PCB REV. B ONLY.
3/8/82



NOTE : FOR PCB REV. B ONLY
3/8/82.

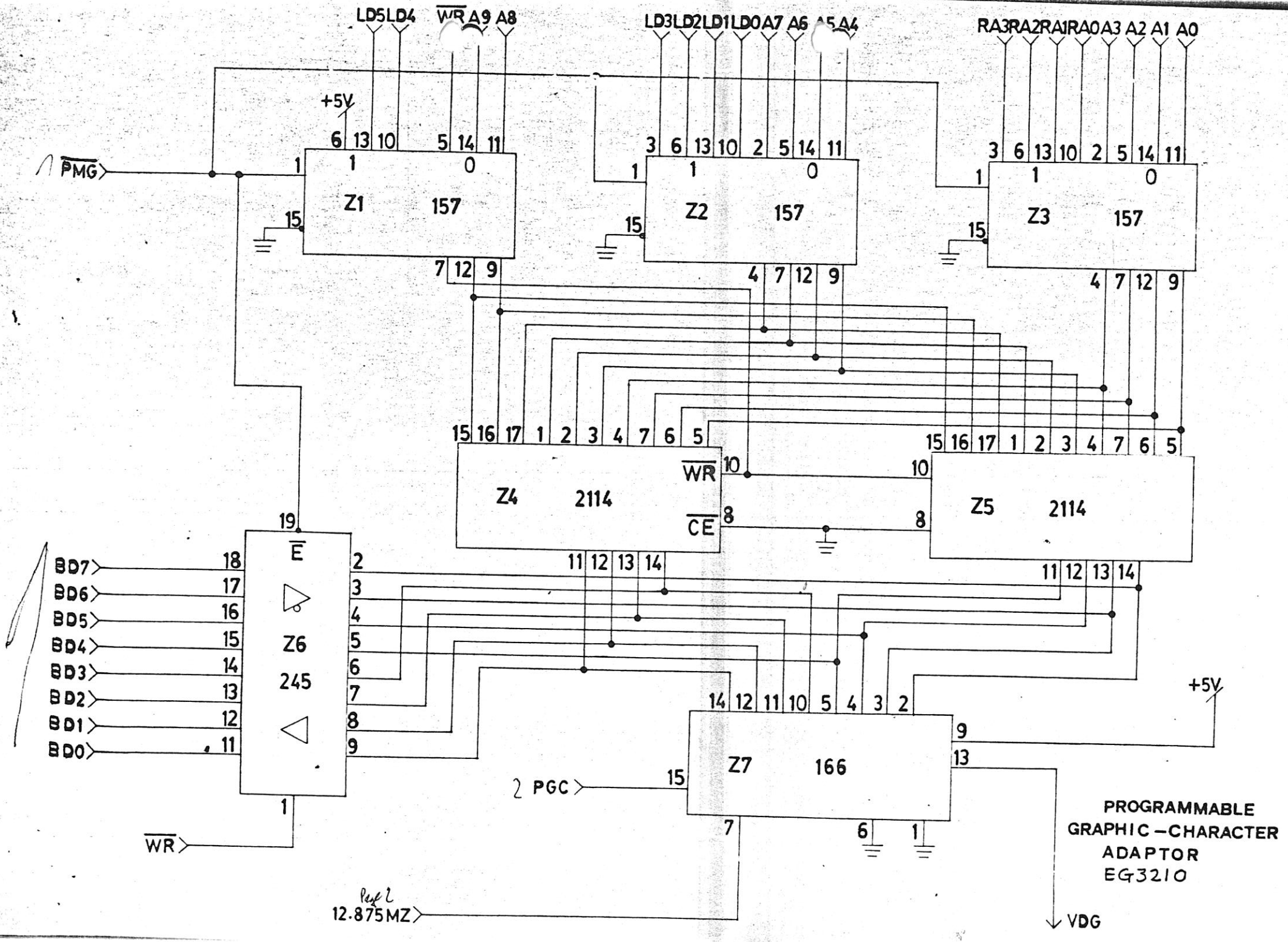


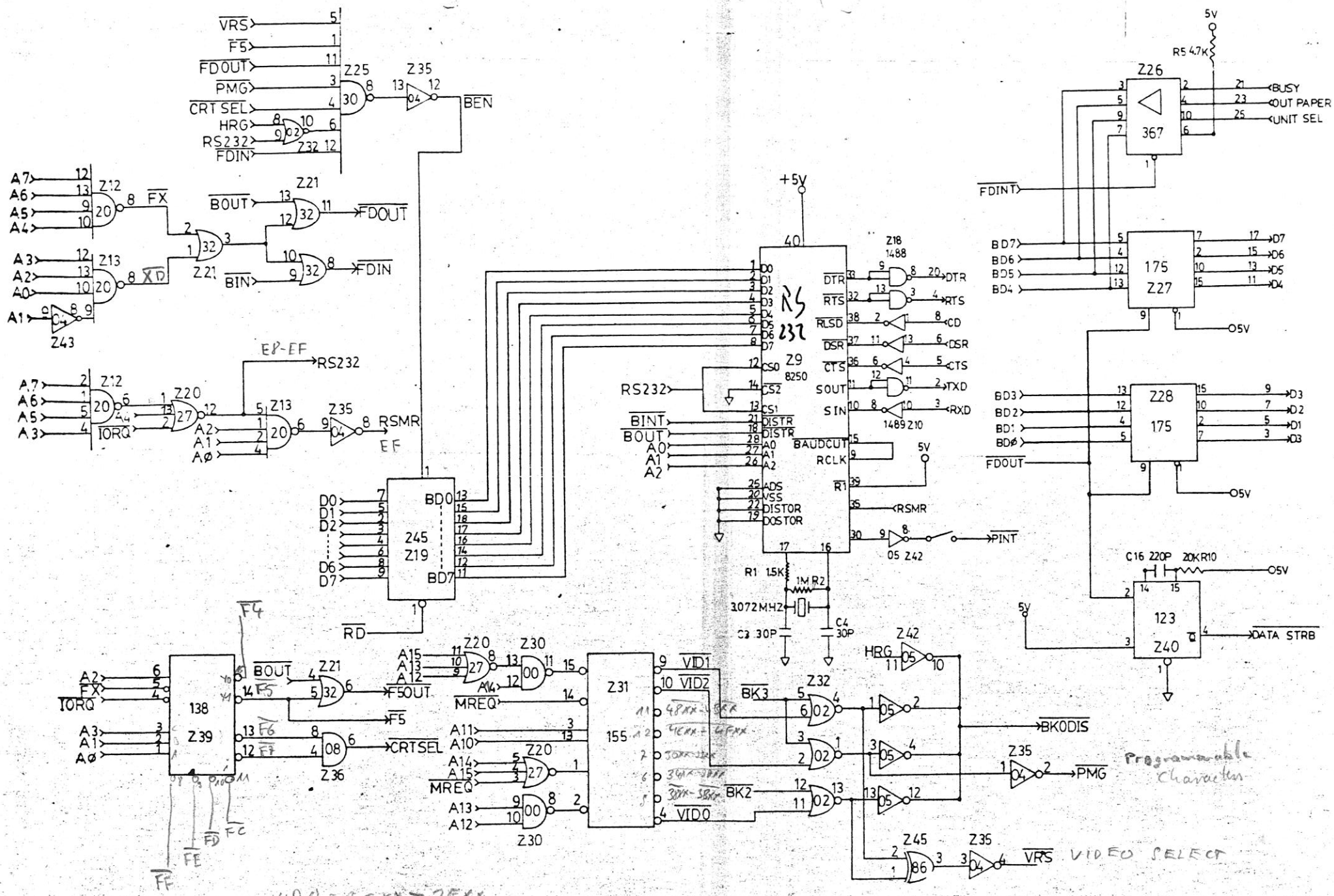
NOTE: FOR PCB REV. C
UPDATED CIRCUIT.
3/8/82



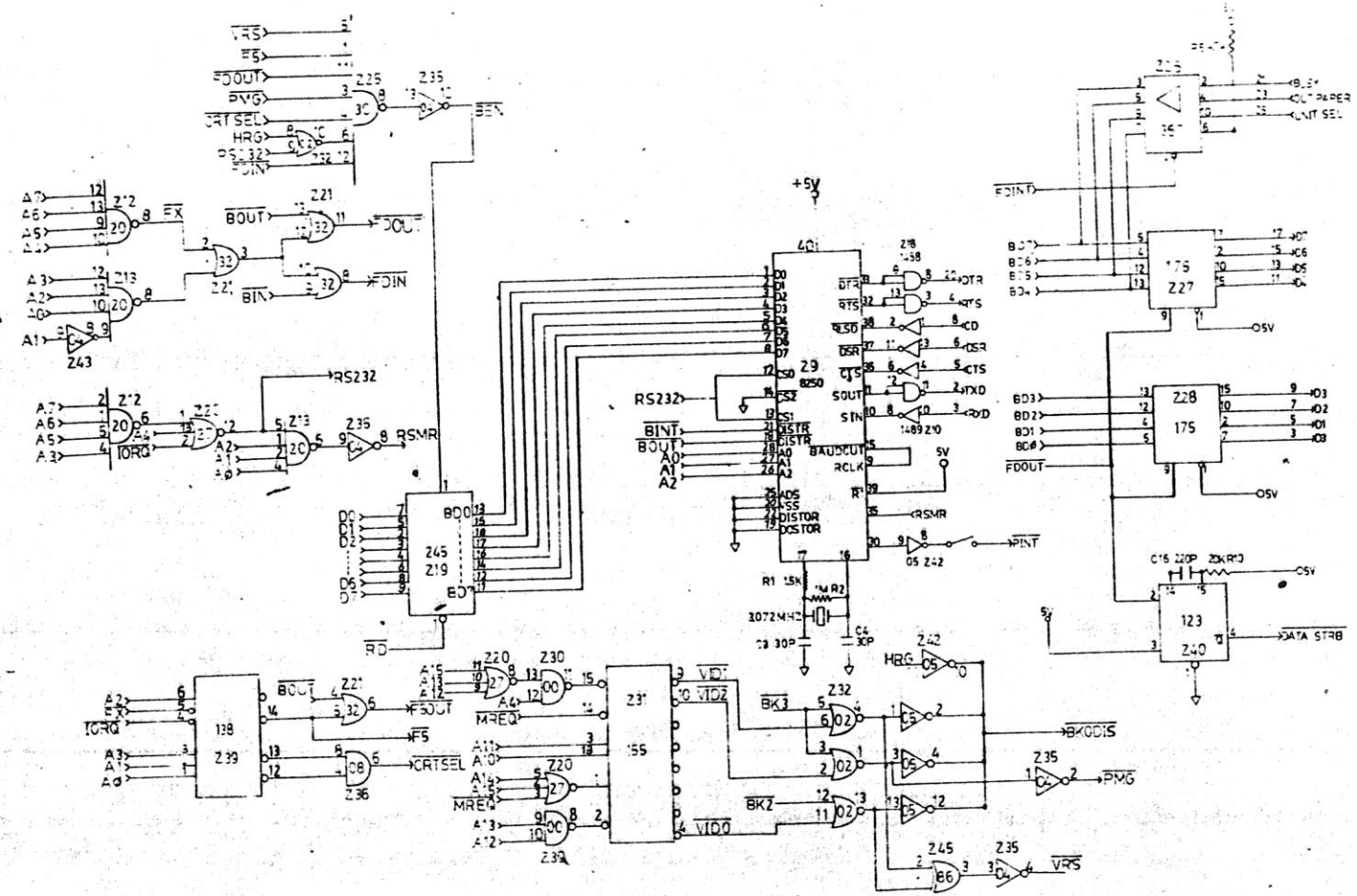
POWER SUPPLY
EG3200
PAGE 2

NOTE : FOR PCB REV. C
UPDATED CIRCUIT
3/8/82.


LD5 LD4 WR A9 A8
LD3 LD2 LD1 LD0 A7 A6 A5 A4
RA3 RA2 RA1 RA0 A3 A2 A1 A0
+5V
PMG
Z1 157
Z2 157
Z3 157
Z4 2114
Z5 2114
WR
CE
Z6 245
E
BD7
BD6
BD5
BD4
BD3
BD2
BD1
BD0
WR
Z7 166
PGC
12.875MZ
+5V
VDG
PROGRAMMABLE
GRAPHIC – CHARACTER
ADAPTOR
EG3210



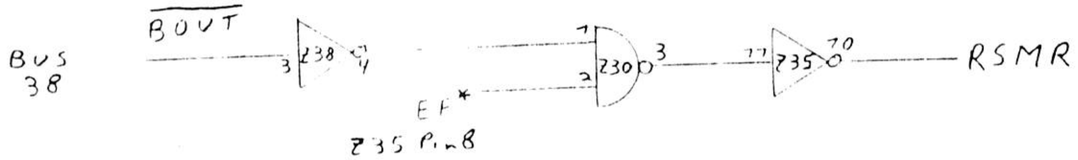
INTERFACE 1
PAGE 1 OF 2



INTERFACE 1
PAGE 1 OF 2

$RSMR = BOUT \cdot EF^* = \overline{\overline{EF^*} + \overline{BOUT}}$

$= \overline{\overline{\overline{BOUT} \cdot EF^*}}$

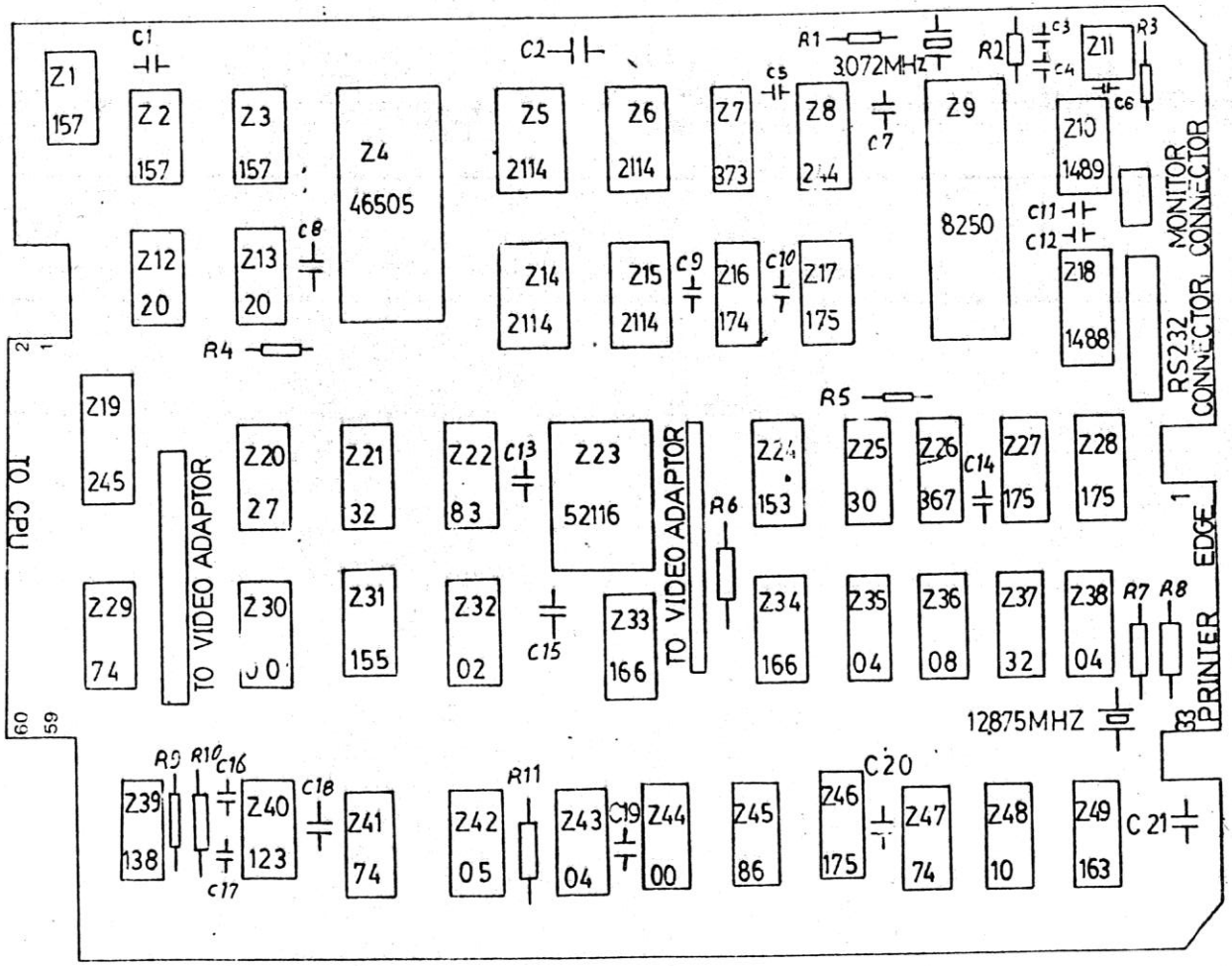


Genie III Interface I (Unterste Platine: Druckeranschluß)

Die Hardware modifikation verhindert ein RESET des seriellen Bausteins INS 8250, wenn die unteren Adress-leitungen EF beinhalten und IORQ in der CPU anliegt. Dieses Zusammentreffen ist gegeben, wenn der 25ms Interrupt in einer Adresse xxEF auftritt.
Nach der Modifikation ist ein RESET des Bausteins mit OUT (EF), 3 möglich

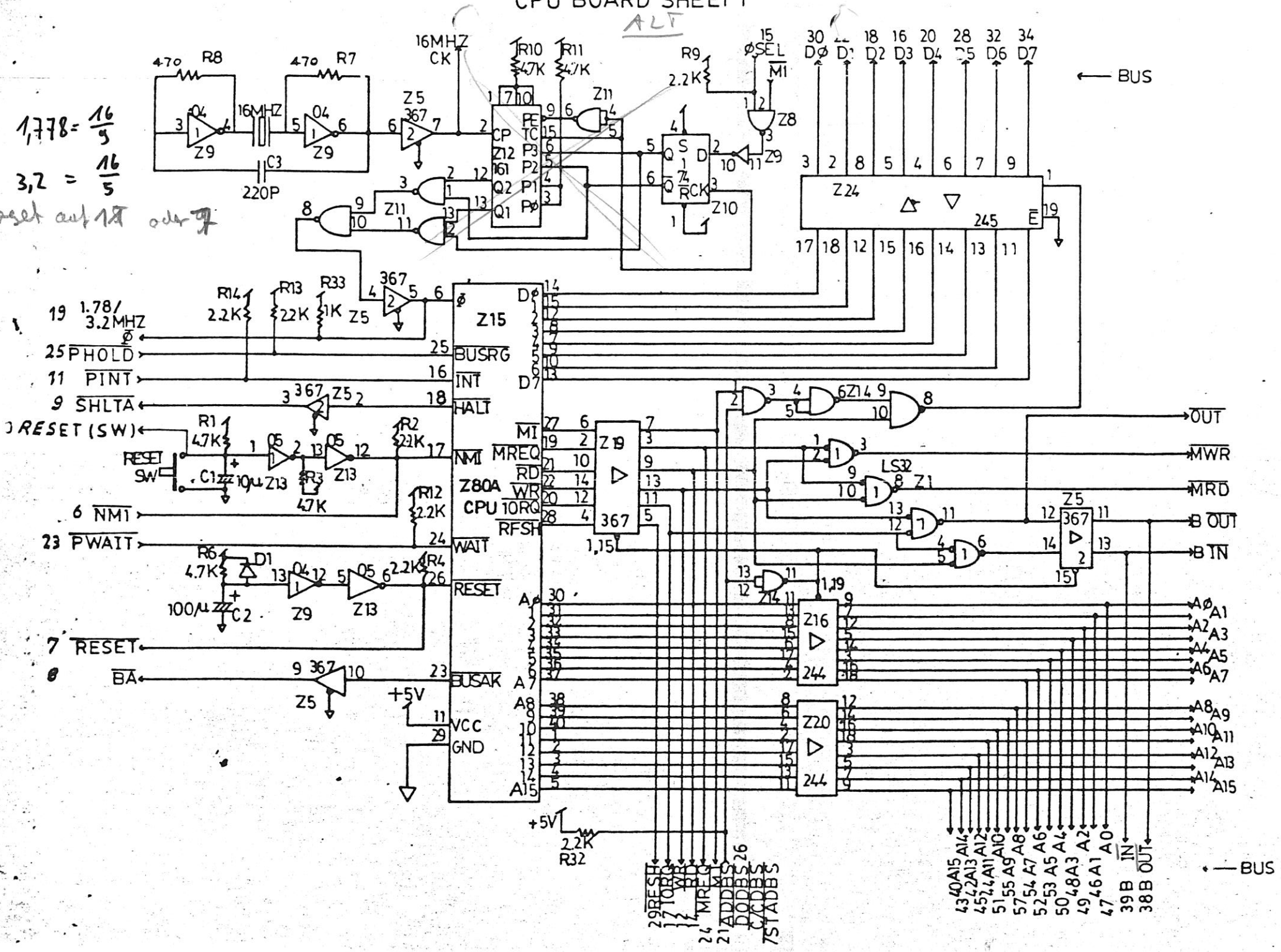
Bitte EACA benachrichtigen

J.Heise 09.05.83



GENIE III INTERFACE 1

CPU BOARD SHEET 1



Nummer Beschreibung

GBVIT2 III + Card

IC 1,2,12	74LS157
IC 3	74LS30
IC 4	82S123 oder aehnlich PROM 32*8 Tri-State
IC 5	74LS74
IC 6,8,10,16 17	74LS32
IC 7	7407
IC 9	74LS00
IC 11	74LS174
IC 13	74LS245
IC 14,15	74LS138
IC 18	74LS293
IC 20,23	75189
IC 22,24	INS 8250
IC 21,25	75188
IC 26	74LS374
IC 27	74LS367
IC 28	74LS123

Bank 1:	
IC69-IC76	4164 150ns ohne self refresh
Bank 2:	
IC53-IC60	4164 150ns ohne self refresh
Bank 3:	
IC37-IC44	4164 150ns ohne self refresh
Bank 4:	
IC61-IC68	4164 150ns ohne self refresh
Bank 5:	
IC45-IC52	4164 150ns ohne self refresh
Bank 6:	
IC29-IC36	4164 150ns ohne self refresh

384 K

R1-R16	33 Ohm 1/8W
R17	1.0 kOhm 1/8W
R18,R20	1 MOhm 1/8W
R19 R21	1.5 kOhm 1/8W
R22	20 kOhm 1/8W
D	TD68 o.ae.
Q	3.072 MHz
C	0.1 uF
C1-C4	30 pF ker.
C5	220 pF

Inhalt des PROM's:

Adresse	Daten
00-0C	EF
0D	FF
0E	ED
0F	EB
10	E7
11-1F	EF